TEL AVIV UNIVERSITY

The Iby and Aladar Fleischman Faculty of Engineering
The Zandman-Slaner School of Graduate Studies

Capacitively Isolated Quasi-Resonant LED Drivers

A thesis submitted toward the degree of
Master of Science in Electrical and Electronic Engineering

by

Alexander Bazarov

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This research was carried out in The School of Electrical Engineering
The Department of Electrical Engineering – Physical Electronics
Under the supervision of Dr. Alexander Abramovitz
and Prof. Doron Shmilovitz

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In memory of my grandparents: Faina and Bair Bazarov, Frida and Artem Kozlov.

ABSTRACT

During the last decade, there is a rise in popularity of light emitting diodes (LEDs) lighting. The rise is a result of many advantages of LEDs such as reduced energy consumption, long lifetime, and being environment-friendly. With rising demand for LEDs grows demand for LED drivers that convert AC line voltage to current controlled DC output suitable for LEDs.

There is a long list of desired LED driver qualities: high efficiency, long lifetime, high power factor and low harmonic distortions, possibility to drive a high number of LEDs from a single LED driver and all this with safety protections and for a low cost. One of the possible ways to address many of the requirements is to reduce the number of stages in energy conversion process inside LED driver by combining them.

Present work analyses family of Quasi-Resonant LED Drivers by deriving major performance indexes theoretically and evaluating them by both simulation and experiment. This family combines power factor correction (PFC) stage with power conversion and current balancing into a single stage. Also, this stage adds capacitive isolation barrier between primary line circuits and secondary outputs toward the LEDs, simplifying protection against electric shock.

The analyzed family of LED drivers has additional advantageous merits including small parts number, single ground referenced switch with non-isolated ground referenced gate driver. Isolation capacitors are part of resonant circuits with both input and output inductors causing soft switching of all semiconductors. Quasi-Resonant operation with constant switch on-time and discontinuous conduction mode causes resistive input characteristic, and as a result, power factor is close to unity, and harmonic distortions also are small.

Built prototypes matched to theory and simulation. Power factor was above 0.99 and Total Harmonic Distortion below 5% at max working points supplying near 20W per LED string.

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LIST OF ABBREVIATIONS AND SYMBOLS

AC	-	Alternating Current
ω_{0i}	-	Angular Resonant Frequency of the L_i-C_s branch
ω_{0r}	-	Angular Resonant Frequency of the L_r-C_s branch
C_B	-	Bank Capacitor
X_{base}	-	Base quantity (X), e.g. I_{base} is base current.
Z_{0i}	-	Characteristic Impedance of the L_i-C_s branch
Z_{0r}	-	Characteristic Impedance of the L_i-C_s branch
COB	-	Chip On Board
CM	-	Common Mode
CCD	-	Coupled Current Doubler
CD	-	Current Doubler
DC	-	Direct Current
V_{ds}	-	Drain-Source Voltage across a switch
η	-	Efficiency
η_{Sx}	-	Efficiency of stage x
EMI	-	Electromagnetic Interference
ELV	-	Extra Low Voltage
HID	-	High Intensity Discharge
r^2	-	Inductors ratio (Input/Resonant)
D_i	-	Input Diode
L_i	-	Input Inductor
t_x	-	Length of state A
LED	-	Light Emitting Diode
C_L	-	Load Capacitance
R_L	-	Load Resistance
V_L	-	Load Voltage
MRCIC	-	Multi-Resonant Capacitively Isolated Converter
m_c	-	Normalized Capacitor Voltage
j_i	-	Normalized Input Inductor Current
X_n	-	Normalized quantity (X) by base quantity, e.g., I_n=I / I_{base}

j_r	-	Normalized Resonant Inductor Current
OLED	-	Organic LED
D_o	-	Output Diode
η_o	-	Overall efficiency
V_m	-	Peak Capacitor Voltage
PFC	-	Power Factor Correction
QRLEDD	-	Quasi-Resonant LED Driver
L_r	-	Resonant Inductor
RMS	-	Root Mean Square
SELV	-	Safety Extra Low Voltage
C_S	-	Series Capacitance
SSL	-	Solid-State Lighting
T_{on}	-	Switch on-time
f_s	-	Switching Frequency
T_s	-	Switching Period
t_i	-	Time at point i
TC	-	Touch Current
ZC	-	Zero Current
ZV	-	Zero Voltage

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CHAPTER 1

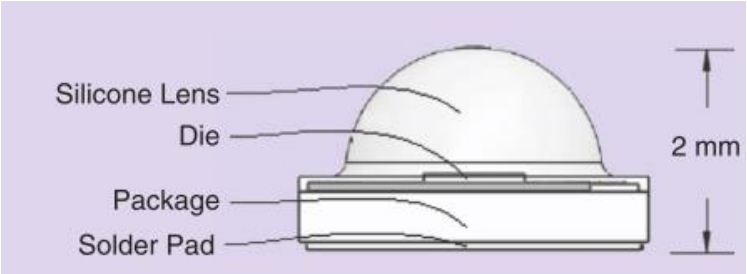
INTRODUCTION, RESEARCH OBJECTIVES, AND WORK STRUCTURE

1.1. INTRODUCTION

From a variety of available light sources, a Solid-State Lighting (SSL) that contains Light Emitting Diodes (LEDs) and Organic LEDs (OLEDs) looks very advantageous compared to other light sources like fluorescent, High-Intensity Discharge (HID), Incandescent, etc. According to the goals of the U.S. Department of Energy, switching to SSL could reduce the lighting energy use of the USA by 75 percent in 2035 [1]. In addition to energy efficiency, SSL sources have longer lifetime increasing savings on maintenance costs. LEDs do not contain a bulb, filament, glass, and gasses making them compact and vibration resistant and do not contain mercury making them safer for the environment [2], [3].

A typical LED structure and photo may be seen in Fig. 1.1. In comparison to incandescent lamps that may be directly connected to available DC or AC power sources of matching V_{rms} value, LEDs require small DC voltage to operate. This requires usage of LED drivers as power converters from the supply AC line to match it to LEDs (e.g., 3V, 350mA).

To increase luminous flux and decrease high step-down ratio LEDs are usually connected serially into strings. This decreases reliability as one LED failure may cause an entire string to turn off. This problem may be solved partially using an active bypassing component. These devices are connected in parallel to each or a group of few LEDs. When a LED fails it shorts out the group containing failed LED. This bypass makes other LEDs operational [4], [5].



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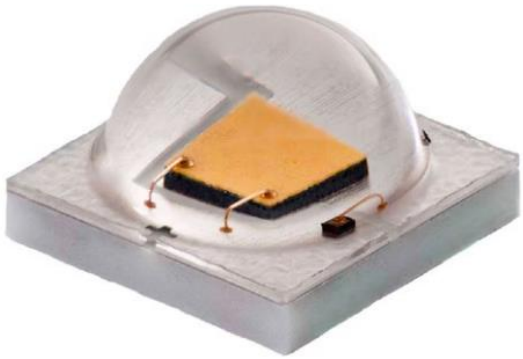
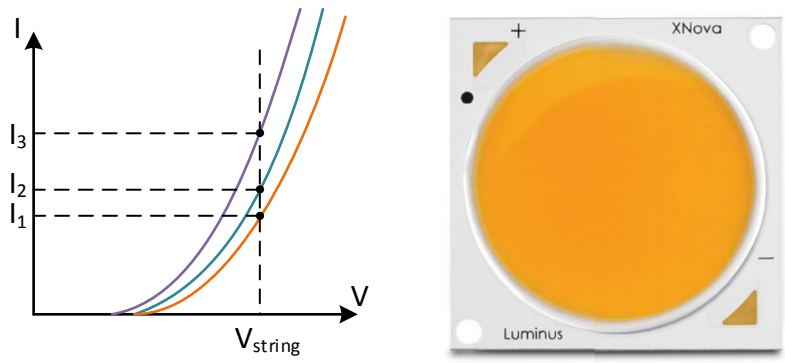


(b)

Fig. 1.1. (a) Typical LED structure [3]; (b) Photo of a commercially available LED [6].

To further increase luminous flux and keep string voltage in the desired range, a parallel connection of strings is used. This creates a problem of current balancing since sharp V-I LED characteristics causes big current variations between strings, see Fig. 1.2 (a). Various current balancing methods exist to address this problem: active current balancing using a linear or switching technique, passive methods using passive components in series with strings [7]. Another method is closely matched LEDs in a thermally coupled module with various series-parallel connecting combinations keeping current imbalances in an acceptable range, e.g. Chip On Board (COB) packages, see Fig. 1.2 (b). However, connecting such modules in parallel still requires the usage of same current balancing methods.



(a) (b)

Fig. 1.2. (a) LED strings V-I characteristics; (b) Matched LEDs grid in thermally coupled Chip On Board (COB) package [8].The LEDs themselves are hidden behind a yellow phosphorus layer.

A typical offline LED driver structure is shown in Fig. 1.3. It usually consists of the following stages:

- Electromagnetic Interference (EMI) filter – limits radio frequency noise produced by the LED driver to meet regulations in place (e.g., IEC 61000-4-3 [9]).
- PFC / Rectifier – limits input current harmonics (e.g. to meet IEC 61000-3-3 [10]).
- Power Converter – performs the step-down conversion and controls the output voltage and current.
- Rectifier / Current Balancer –rectifies voltage of power converter and in case of multiple strings controls current balance.

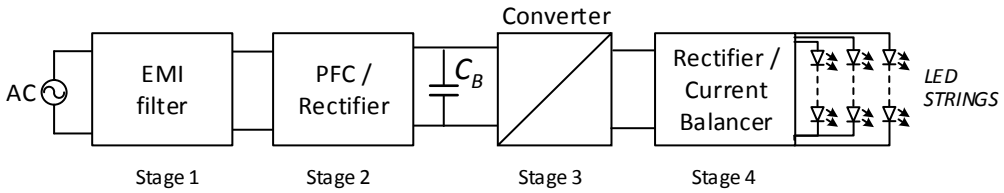


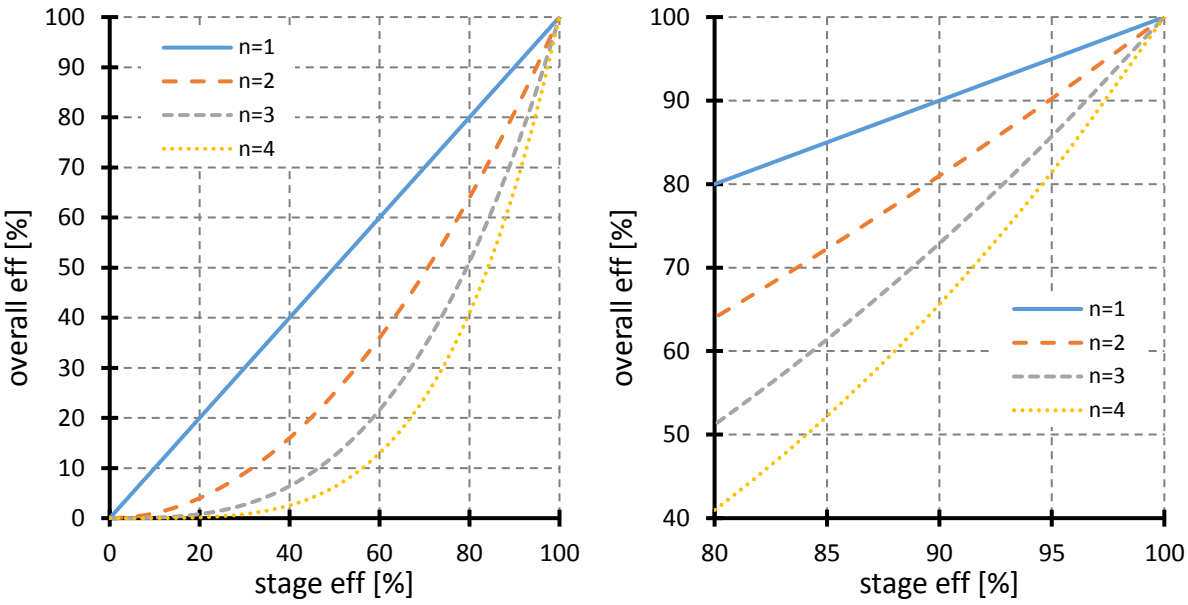
Fig. 1.3. A typical block diagram of the offline power converter for driving light sources consisting of Electromagnetic Interference (EMI) filter, power factor corrector (PFC), power converter, rectifying and/or current balancing stages.

In addition to the mentioned stages, there is usually a bank capacitor between the PFC and Converter stages. It helps smooth double line-frequency ripple at the output and reduces required capacitors at the output. The short life of electrolytic capacitors becomes an issue compared to the long life of the LEDs themselves. Allowing a higher ripple at the input of the Converter stage enables to switch from high capacity electrolytic capacitors to more reliable ceramic and film capacitors but having the lower capacity [11].

For a multi-stage power converter, overall converter efficiency, η_O, may be calculated as a multiplication of stage efficiencies, η_{Sx}, where x is a stage index. In the case where every stage has the same efficiency, η_S, then the overall efficiency becomes:

$$\eta_o = \eta_{S1}\eta_{S2} \ldots \eta_{Sn} = \eta_S^n \qquad (1.1)$$

Therefore, the overall efficiency decays exponentially with the number of stages, see Fig. 1.4. For example, four stages with an efficiency of 95% each, will give an overall efficiency of just slightly above 80%. Decreasing the number of stages gives a possibility to increase efficiency, reduce the number of components and hence the size and price of the driver.



(a) (b)

Fig. 1.4. Overall efficiency of power converter as a function of stage efficiency for different number of stages: (a) full range; (b) zoom-in from 80% to 100%

The LED drivers may be products by themselves, be part of luminaries or part of any other product. To be safe and legally permitted for the use they must meet safety requirements that usually vary slightly between countries but are mainly based on International Electrotechnical Commission (IEC) standards. In the case of LED drivers, it may be IEC 61347 – "Lamp Controlgear" for drivers themselves [12], IEC 60598 "Luminaires" when they are part of luminaires [13] and in the case when LED drivers are part of other products IEC 60065 and IEC 60950 are used (undergoing combining and replacing with a newer IEC 62368 standard [14]). To meet these requirements, an isolated output voltage within Safety Extra Low Voltage (SELV) limits will cause equipment to be class III with no requirements for additional protection against electric shock on the secondary side [15] giving maximal simplicity and flexibility for product designers avoiding the need for double insulation or

grounded enclosure. This gives the motivation to use ELV voltage levels at the output and implement isolation causing driver to be with SELV protection.

Isolation means no direct contact between the primary input and slave output conductors. Isolation is usually assigned by using a magnetic transformer although different methods exist. For example piezoelectric transformers [16] or small series capacitors [17] that also prevent direct contact.

An idea of isolation by series of capacitors utilizes the fact that even a magnetic transformer has parasitic stray capacitance between isolated windings. Moreover, primary and secondary windings are usually bridged with class Y capacitors to reduce EMI [15].

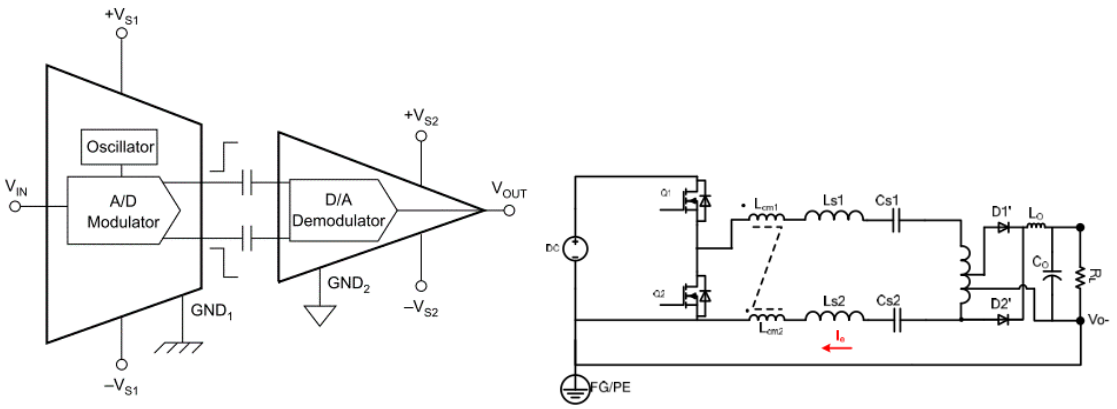
Due to the various methods and parameters of isolation, to test overall protection efficiency, IEC 60990 defines Touch Current (TC) and the method of its measurement. Other standards give limits on TC as the main factor that puts a human at risk of an electric shock. TC is measured on the final product to meet safety requirements. Therefore, the magnetic transformer may be replaced by the use of small series capacitors certified as class Y and meet requirements on TC.

In current work, a family of topologies that combine PFC, Power Converter and Current Balancer will be analyzed and verified by the simulation and experiment. Power converters will be based on capacitive isolation and output will be in SELV range.

1.2. LITERATURE SURVEY

A method of capacitive isolation is well known in the field of data transfer and isolation amplifiers [18]–[22]. The method is based on the usage of a pair of small capacitors on the "go" and "return" bus lines, blocking DC and low frequencies and allowing for high frequencies to pass, see Fig. 1.5 (a).

Barbehenn and Elgee, 1996 [17] and Bäurle, Matthews, Saint-Pierre, 2008 [23] have patented power converters with capacitive isolation replacing bulky magnetic isolation transformers [24]–[26]. Zhu, Xu, Sun and Wang, 2010 [27] proposed to add resonant inductors in series with isolation capacitors to further decrease their combined impedance and allow higher power transfer at near resonance frequencies. In addition, they proposed common mode (CM) choke at L-C lines or DC bus to further decrease TC, see Fig. 1.5 (b).

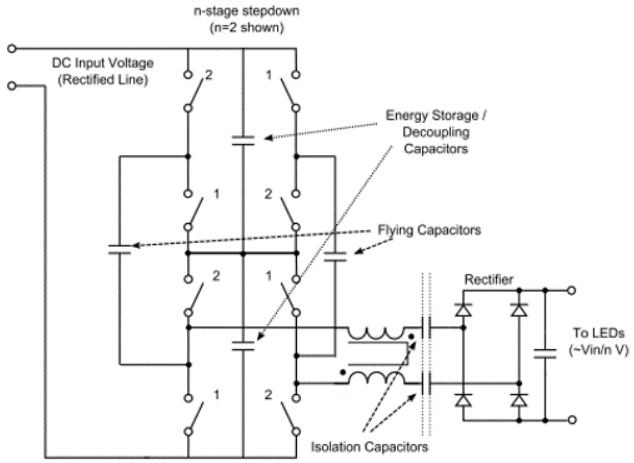


(a) (b)

Fig. 1.5 Capacitive isolation (a) Example of usage in isolation amplifier [20]; (b) Usage in power conversion with added series inductors to reduce impedance at the resonant frequency by Zhu *et al.*, 2010 [27].

Common mode choke usually exists as a part of EMI filter at AC line input into driver [28], so it may be utilized as TC limiter without adding additional CM choke to following LED driver stages from Fig. 1.3. Moreover, this is the reason why EMI filter may influence TC measurements.

Looking at the application of capacitive isolation in LED drivers, Kline, Izyumin, Boser, and Sanders, 2012 [29] proposed a switched capacitor circuit to generate a high frequency for power transfer via isolation capacitors with a resonant inductor, see Fig. 1.6 (a). Moreover, further Le, Kline, *et al.*, 2013 [30] expanded this topology to a stackable multi-level converter to handle high voltages with integrated circuit implementation. Resonant inductors are also utilized to achieve zero voltage switching (ZVS) on switches enabling MHz range operation. The topology requires PFC circuit at the input.



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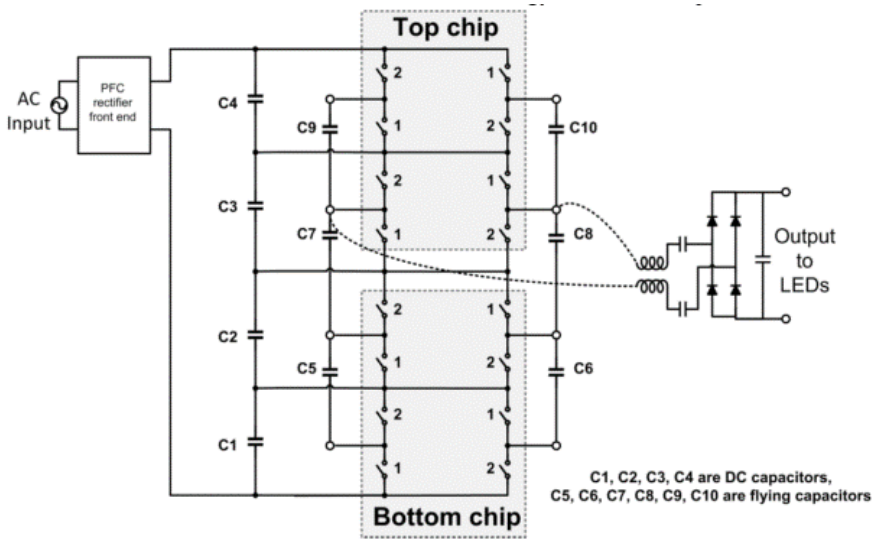


(b)

Fig. 1.6 (a) Proposed topology by Kline *et al.*, 2012 [29]; (b) Stackable expansion by Le *et al.* [30]

Eloi, Sa, Dos Santos, Miranda, and Antunes, 2015 [31] proposed a topology as seen in Fig. 1.7. By disconnecting Cs1, it will give the same half-bridge with isolation scheme as in Fig. 1.5 (b) (here bottom isolation capacitor is divided into two which are connected to both DC rails). Resonant inductor, Lo, is moved after the rectifier. This circuit has resistive input characteristics by operating in quasi-resonant mode keeping Lo in discontinuous conduction mode (DCM). Li-Ci used to filter out switching frequency. Hence, this topology combines PFC stage with power conversion.

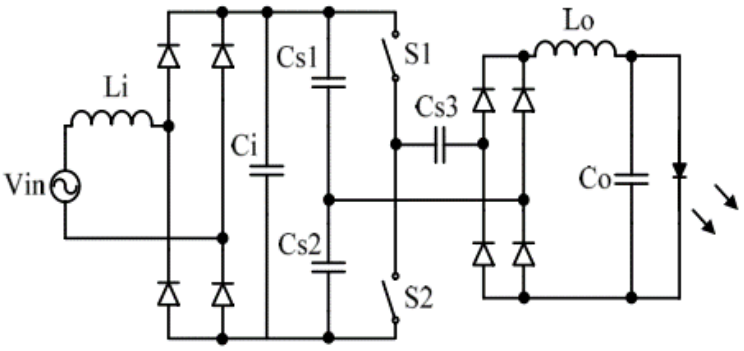


Fig. 1.7 Proposed topology by Eloi *et al.*, 2015 [31]

Zhang, Wang, and Wu, 2012 [32] expanded Zhu *et al.*, 2010 [27] to drive multi-string LEDs, see Fig. 1.8. The proposed topology uses additional PFC stage; switches operate at above resonance frequency.

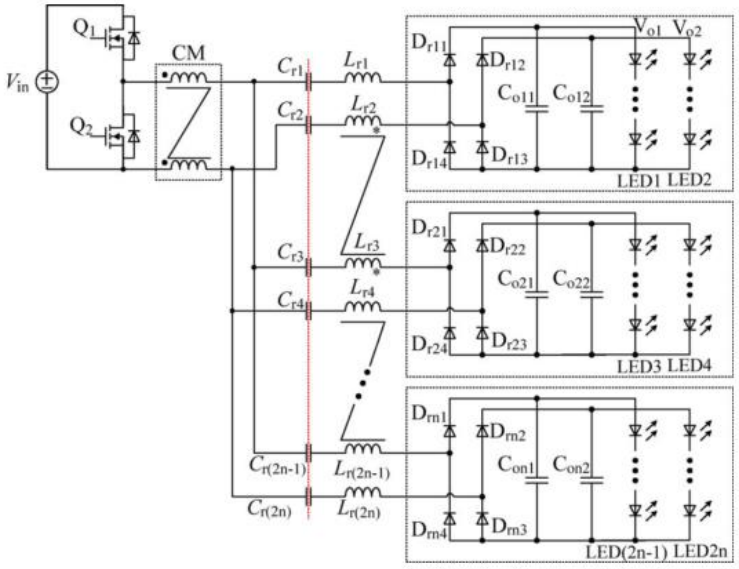


Fig. 1.8 Proposed topology by Zhang *et al.*, 2012 [32]

Looking at the LED drivers described above, all of them require at least two switches and a floating gate driver. They use full bridge rectifier requiring four diodes at the output. Zhang *et al.*, 2012 [32] and Kline *et al.*, 2012 [29] also require additional PFC stage.

Shmilovitz, Ozeri, and Ehsani, 2014 [33] proposed a topology that combines PFC and power conversion stage and uses a single diode as a rectifier, see Fig. 1.9. This topology operates in ZVS at both turn-on and turn-off of the switch in continuous conduction mode above resonance.

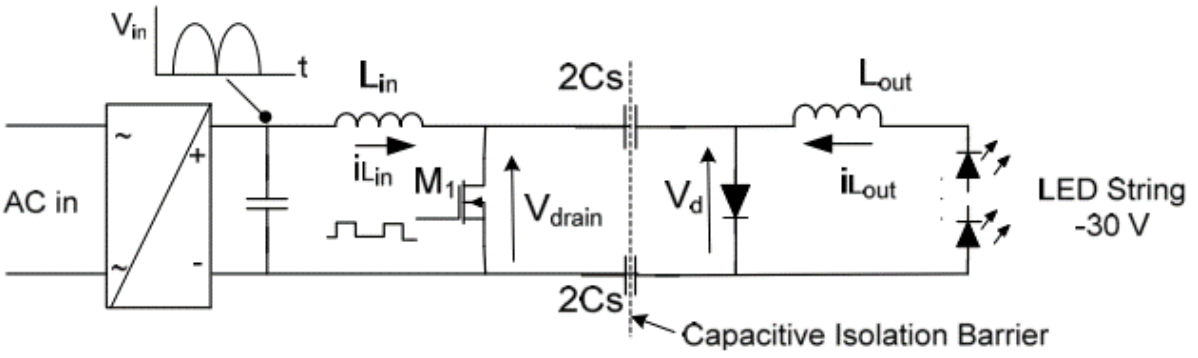
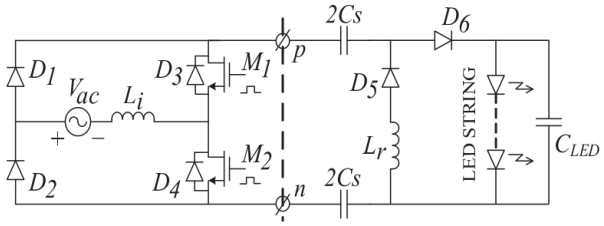


Fig. 1.9 Proposed topology by Shmilovitz *et al.*, 2014 [33]

This topology expanded further into the family of ZCS-ZVS Quasi-Resonant LED Drivers (QRLEDD) by Abramovitz, Reichman, Ehsani and Shmilovitz [34]–[38] see Fig. 1.10 .



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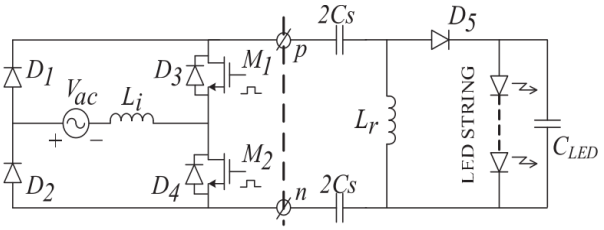

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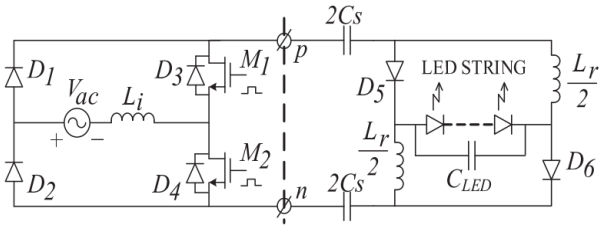

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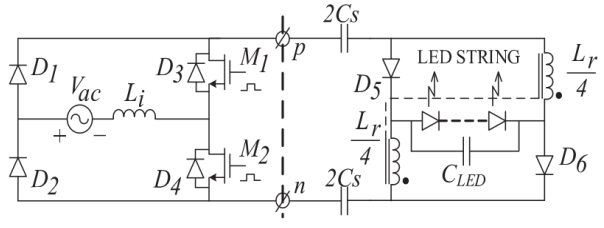

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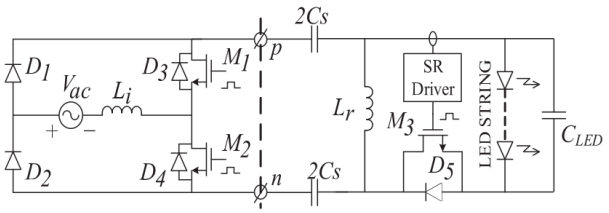

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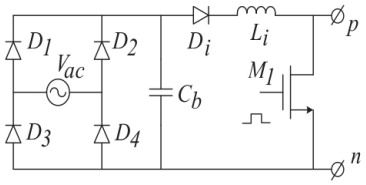

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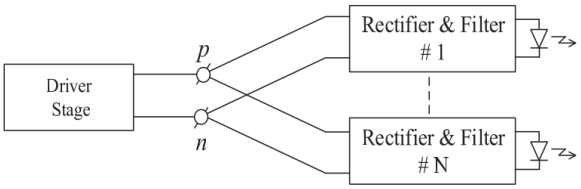


(g)

Fig. 1.10 Previously proposed family of bridgeless (BL) Quasi-Resonant LED drivers (QRLEDD) by Shmilovitz *et al.*, 2016 [38]: (a) basic BL-QRLEDD; (b) modified BL-QRLEDD; (c) current doubler rectifier (CD) CD BL-QRLEDD; (d) coupled current doubler (CCD) CCD BL-QRLEDD; (e) BL-QRLEDD with synchronous rectifier; (f) single-switch front-end for QRLEDD; (g) general concept of the multi-string QRLEDD.

Analyses of all presented topologies using bridgeless (BL) front-end or using single-switch front-end from Fig. 1.10 (f) are identical as they are done in the vicinity of a constant input voltage. The topology from Fig. 1.10 (a) is analyzed in Abramovitz *et al.*, 2015 [35] and Shmilovitz *et al.*, 2015 [36]. Modified QRLEDD from Fig. 1.10 (b) analyzed in Reichman, 2015 [37].

This family has low components count, combined PFC, and converter stages. Using single-switch front end from Fig. 1.10 (f) only a single ground referenced gate driver is needed. Also, a proposed expansion to multi-string, Fig. 1.10 (g), is much simpler than in Fig. 1.8.

This work continues the analysis of proposed topologies from Fig. 1.10 with the aim to finish analytic analysis, derive design procedures and build prototypes to verify theory and simulations.

1.3. RESEARCH OBJECTIVES AND WORK STRUCTURE

This work continues analysis of the converters family proposed by Shmilovitz *et al.*, 2016 [38], see Fig. 1.10 . In previous analyses [35]–[37] principal characteristics are derived without getting full analytical waveforms of currents and voltages. Also, not all proposed converters were analyzed.

Chapter 2 completes a state-plane analysis of Fig. 1.10 (b) as the basis for following topologies and plots full trajectories of all states in state-planes. Additional performance indices derived and some refinements applied. The results have been submitted for publication consideration under the name "State-Plane Analysis of Capacitively Isolated Multi-Resonant Converter."

Chapter 3 deals with an extension of topology from the first part to multi-string version as predicted by Fig. 1.10 (g). A method to analyze multi-string configurations developed, simulated and tested by experiment on modified QRLEDD. The results were presented at OPTIM-ACEMP 2017 conference [39] and more detailed version, "Multi-String Capacitively Isolated Quasi-Resonant LED Driver," has been submitted for publication considerations.

Chapter 4 deals with Current Doubler (CD) and Coupled Current Doubler (CCD) rectifier topologies from Fig. 1.10 (c) and (d). Topologies are analyzed, showing their equivalency, and the analysis is verified by simulation and experiment on CCD version. The results were presented at the European Conference on Power Electronics and Applications 2016 (EPE'16) [40].

Chapter 1 – Introduction, literature survey, research objectives and work structure.

Chapter 2 – Modified QRLEDD [37] from Fig. 1.10 (b) expanded and refined analysis, simulation and measurements results.

Chapter 3 – Method of extension single-string topology to multi-string, an example of analysis and experiment results of Modified QRLEDD topology.

Chapter 4 – CD and CCD QRLEDD topologies and their analysis, simulation and measurements results.

Chapter 5 – Concludes the thesis and suggests future work.

CHAPTER 2

MULTI RESONANT CAPACITIVELY ISOLATED CONVERTER

2.1. INTRODUCTION

This chapter continues and completes the analysis of Modified QRLEDD by Reichman, 2015 [37] looking at its topology as a DC-DC Multi Resonant Capacitively Isolated Converter (MRCIC). Equations of voltages and currents of all resonant components are derived applying the State-Plane approach. Trajectories of states are plotted in 2D and 3D. Key characteristics are derived. The analysis is verified by simulation and experiment. This chapter has been submitted for publication considerations as "State-Plane Analysis of Capacitively Isolated Multi-Resonant Converter."

2.2. TOPOLOGY OVERVIEW

The topology of the Multi Resonant Capacitively Isolated Converter (MRCIC) is shown in Fig. 2.1. The proposed MRCIC is comprised of the input inductor, Li, switched by the power switch, M. The input diode Di, in series with Li assures unidirectional energy flow. The capacitive isolation barrier is created by a pair of small series blocking capacitors, 2Cs. Energy is temporarily stored and transferred to the output by the inductor Lr. The diode D_o serves as output rectifier. The load R_L is connected across the large output capacitance, C_L, which filters out the switching ripple.

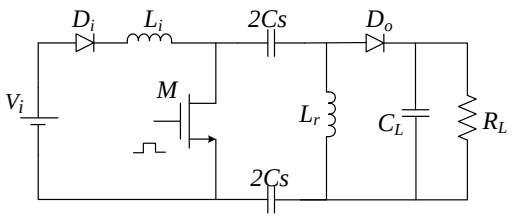
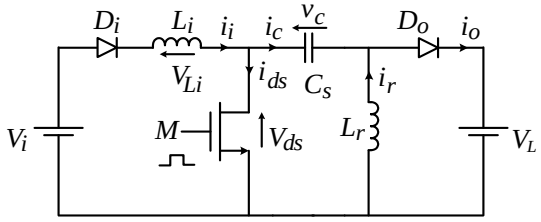


Fig. 2.1. The Multi Resonant Capacitively Isolated Converter.

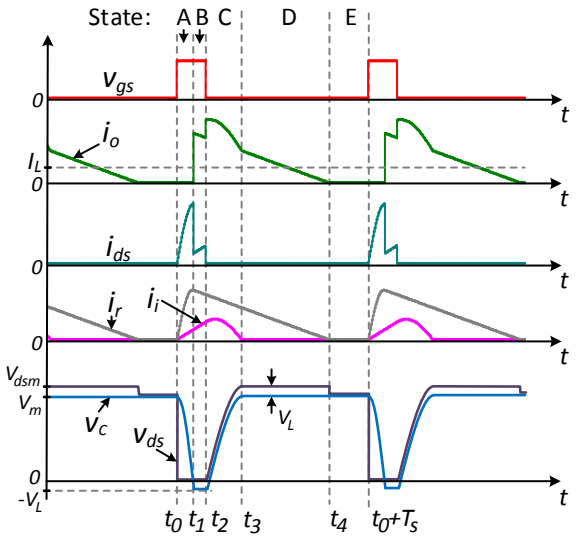
The MRCIC has the advantage of a single ground referenced switch and gate driver. The switch can operate at high frequency due to zero current turn-on and zero voltage switching turn-off conditions inherently created by the circuit. Blocking capacitors are also used as a part of the resonant circuit. Another desirable feature of the MRCIC is its resistive input port characteristics, which stems from discontinuous current mode operation of the input inductor.

2.3. BASIC ASSUMPTIONS

To simplify the analysis the following assumptions are adopted: a) the MRCIC operates in a steady state equilibrium; b) the output voltage across the load, V_L, is regulated by output voltage control loop to a constant value; thus, the large filter capacitance, C_L, can be represented by an equivalent dc voltage sink, V_L; c) the equivalent capacitor, C_s, represents the pair of series blocking capacitors; d) all the semiconductors operate as ideal switches. The resulting model is shown in Fig. 2.2 (a). The detailed steady-state waveforms are presented in Fig. 2.2 (b). Examining the switch waveforms in Fig. 2.2 (b) reveals favorable zero voltage (ZV) turn off and zero current (ZC) turn on switching of the MOSFET switch, which can help to attain high efficiency at high frequency.



(a)



(b)

Fig. 2.2. The proposed MRCIC: (a) simplified equivalent circuit; (b) key simulated waveforms on the switching period scale.

2.4. NOMENCLATURE AND NORMALIZATION

The resonant network of the MRCIC model in Fig. 2.2 (a) is comprised of three switched reactive elements L_i, L_r, and C_s. The switching action reconfigures the network and results in the appearance of multiple resonant frequencies and characteristic impedances. The angular resonant frequency of the L_i-C_s branch is defined as

$$\omega_{0i} = \frac{1}{\sqrt{L_i C_s}} \tag{2.1}$$

while the angular resonant frequency of the L_r-C_s branch is

$$\omega_{0r} = \frac{1}{\sqrt{L_r C_s}} \tag{2.2}$$

Accordingly, the characteristic impedance of the L_i-C_s branch is

$$Z_{0i} = \sqrt{\frac{L_i}{C_s}} \tag{2.3}$$

and the characteristic impedance of the L_r-C_s branch is

$$Z_{0r} = \sqrt{\frac{L_r}{C_s}} \tag{2.4}$$

With the inductor ratio defined as

$$r^2 = \frac{L_i}{L_r} \tag{2.5}$$

the resonant frequencies and the characteristic impedances are related by

$$r = \frac{\omega_{0r}}{\omega_{0i}} = \frac{Z_{0i}}{Z_{0r}} \tag{2.6}$$

(Note that the series equivalent configuration L_i-C_s-L_r does not appear during the normal operation of the circuit, thus, the series equivalent angular frequency $\omega_{0s} = \frac{1}{\sqrt{(L_i+L_r)C_s}}$, and the series equivalent characteristic impedance $Z_{0s} = \sqrt{\frac{L_i+L_r}{C_s}}$ are of no concern here.)

In the following, the voltages in the circuit are normalized with reference to the input voltage, V_i. Hence, the normalized capacitor voltage is defined as

$$m_c(t) = \frac{v_c(t)}{V_i} \tag{2.7}$$

and the normalized load (output) voltage is

$$V_{Ln} = \frac{V_L}{V_i} \tag{2.8}$$

The current through the inductor L_i is normalized according to

$$j_i(t) = i_i(t)/\left(\frac{V_i}{Z_{0i}}\right) = i_i(t)/I_{base} \qquad (2.9)$$

where the base current is defined as

$$I_{base} = V_i/Z_{0i} \qquad (2.10)$$

However, the current through the inductor L_r is normalized according to

$$j_r(t) = i_r(t)/\left(\frac{V_i}{Z_{0r}}\right) = i_r(t)/r\left(\frac{V_i}{Z_{0i}}\right) = i_r(t)/rI_{base} \qquad (2.11)$$

here, (2.6) was used.

The normalized power, P_n, is defined according to

$$P_n(t) = \frac{P(t)}{V_i I_{base}} = \frac{P(t)}{\left(\frac{{V_i}^2}{Z_{0i}}\right)} \qquad (2.12)$$

As usual, the switching frequency is denoted as f_s and is the inverse the switching period T_s, $f_s = 1/T_s$.

The resonant frequency of the L_i-C_s branch (2.1) will be used as a base frequency

$$f_{0s} = \frac{\omega_{0i}}{2\pi} = \frac{1}{2\pi\sqrt{L_i C_s}} = \frac{\omega_{0r}}{2\pi r} \qquad (2.13)$$

Hence the normalized switching frequency, f_n, is

$$f_n = \frac{f_s}{f_{0s}} \qquad (2.14)$$

The base time interval, $T_{base,}$ is defined with respect to the resonant period of the L_i-C_s branch

$$T_{base} = \frac{1}{f_{0s}} = 2\pi\sqrt{L_i C_s} \qquad (2.15)$$

or using (2.1) and (2.6):

$$T_{base} = \frac{2\pi}{\omega_{0i}} = \frac{2\pi r}{\omega_{0r}} \qquad (2.16)$$

Accordingly, the normalized switch on-time is

$$T_{on\_n} = T_{on}/T_{base} = T_{on}\frac{\omega_{0i}}{2\pi} = T_{on}\frac{\omega_{0r}}{2\pi r} \qquad (2.17)$$

2.5. STATES ANALYSIS

Analysis of the MRCIC waveforms in Fig. 2.2 (b) reveals that the high frequency switching cycle of MRCIC is comprised of five topological states. The equivalent circuits of the topological states are shown below in the order of their appearance throughout the switching cycle. The equations for the equivalent circuits can be written and solved for the three state variables $v_c(t)$, $i_i(t)$, $i_r(t)$ in the time domain. The normalized state variable trio

$m_c(t)$, $j_i(t)$, and $i_r(t)$ create a three-dimensional (3D) state-space. Typical 3D normalized solution trajectory of MRCIC is illustrated in Fig. 2.4 (a). The plot was generated by MATLAB computational software. The 3D solution can be projected onto m_c - j_i plane and onto m_c - j_r plane as shown in Fig. 2.4 (b) and (c) respectively. Each such projection creates a two-dimensional state-plane that lends itself to the familiar state-plane analysis technique. This approach translates the three-dimensional problem into a two-dimensional one, which is easier to handle and, for this reason, is adopted here.

2.5.1. STATE A

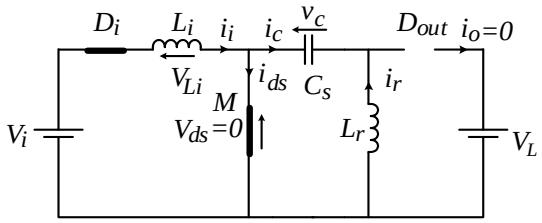


Fig. 2.3. Equivalent circuits of the topological state A.

State A, t_0-t_1, see Fig. 2.3, commences when the switch M is turned on. The turn-on occurs at zero current. Consequently, L_i begins charging from the input source, V_i, via D_i, while C_s and L_r are allowed to resonate.

Examining Fig. 2.2 (b) it is evident that at the start of the switching cycle the capacitor voltage is at its maximum value, V_m, while both inductors carry no current. Therefore, the initial conditions of state A are

$$V_{C0} = v_C(t_0) = V_m \quad (2.18)$$

$$I_{i0} = i_i(t_0) = 0 \quad (2.19)$$

$$I_{r0} = i_r(t_0) = 0 \quad (2.20)$$

Using the equivalent circuit in Fig. 2.3 the normalized solution of state A can be obtained (assuming $t_0 = 0$)

$$m_{CA}(t) = R_r cos(\omega_{0r} t) \quad (2.21)$$

$$j_{iA}(t) = \frac{1}{I_{base}} \frac{V_i}{L_i} \cdot t = \omega_{0i} t \quad (2.22)$$

$$j_{rA}(t) = R_r sin(\omega_{0r} t) \quad (2.23)$$

The normalized solution of state A traces a cosinusoidal arc A in the m_c-j_i plane, see Fig. 2.5 (a), while in the m_c-j_r plane it appears as a circular arc A, see Fig. 2.5 (b), centered at the origin of the plane (0,0) and having a radii R_r

$$R_r = V_{mn} \quad (2.24)$$

That will be determined later on.

State A terminates when

$$v_C(t_1) = V_{C1} = -V_L \qquad (2.25)$$

which in the normalized form is

$$m_C(t_1) = m_{C1} = -\frac{V_L}{V_i} = -V_{Ln} \qquad (2.26)$$

The normalized current through the L_i inductor at the end of state A can be found from (2.22)

$$j_{i1} = j_i(t_1) = \omega_{0i} t_1 \qquad (2.27)$$

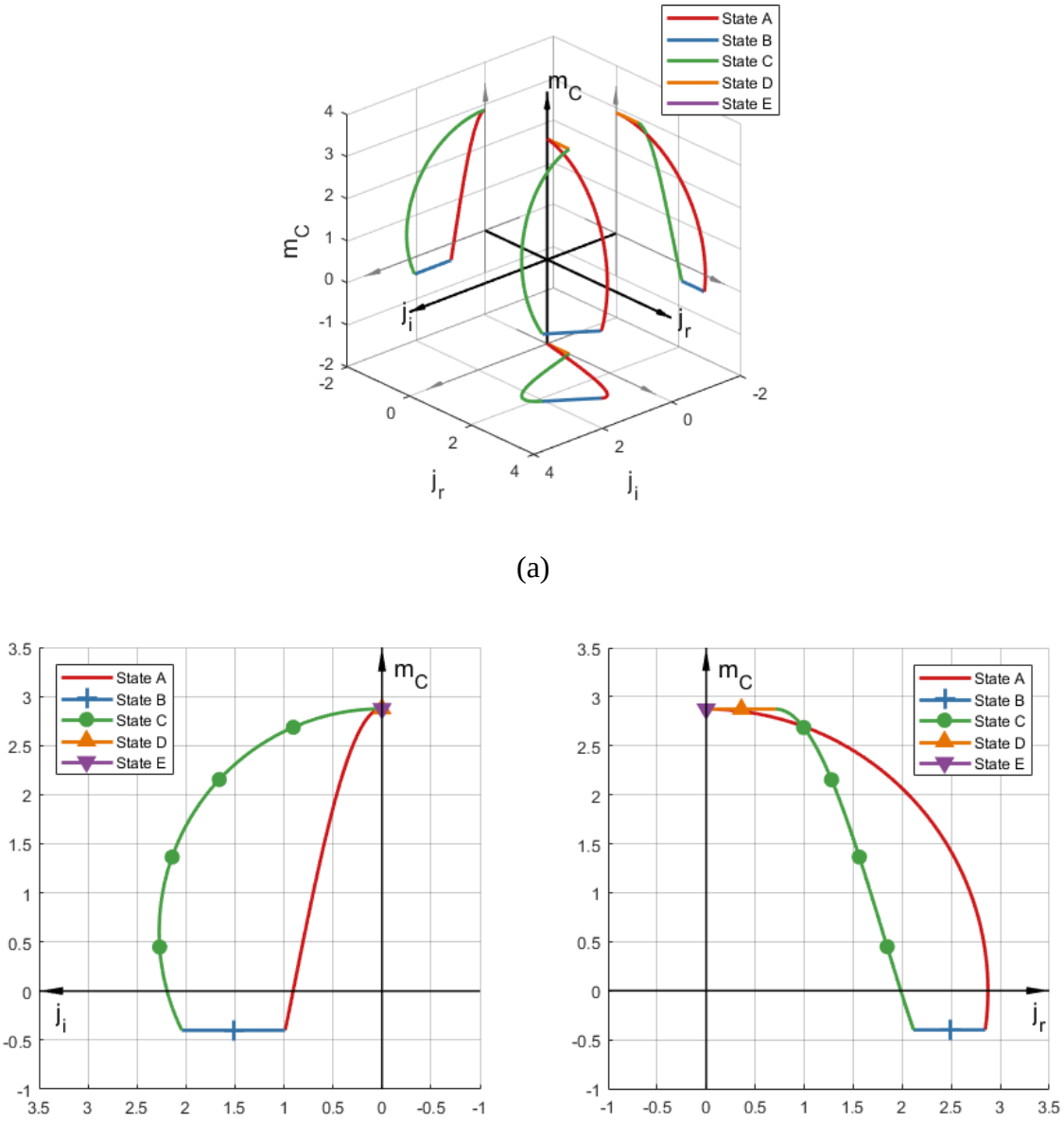
Furthermore, the normalized current through the L_r inductor at the end of state A can be found from Fig. 2.5 (b) applying geometrical considerations

$$j_{r1} = j_r(t_1) = \sqrt{V_{mn}^2 - V_{Ln}^2} \qquad (2.28)$$

Using (2.26) the duration of state A, t_A can be found examining Fig. 2.5 (b) and applying geometrical considerations. Since $t_A = t_1 - t_0$, and since $t_0 = 0$ is assumed

$$t_1 = t_A = \frac{1}{\omega_{0r}}\left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right)\right] \approx \frac{\pi}{2}\frac{1}{\omega_{0r}} = \frac{1}{4r} T_{base} \qquad (2.29)$$

Here, the term $sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right)$ can be neglected in case the peak capacitor voltage is higher than the load voltage so that $V_{mn} > V_{Ln}$.

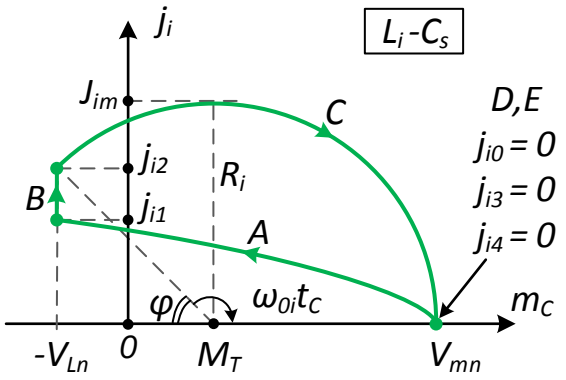


(a)

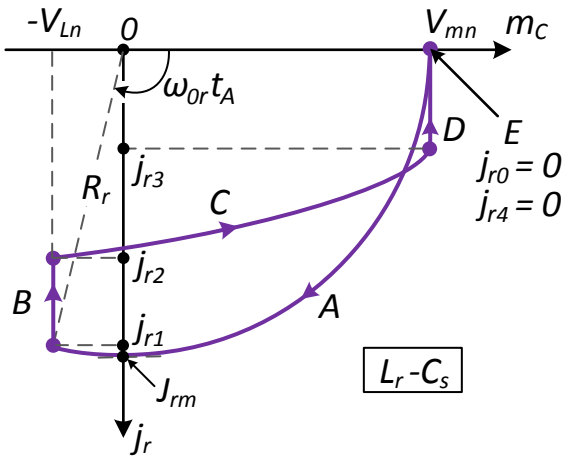
(b)

(c)

Fig. 2.4. MATLAB numerical solution of MRCIC (for $r^2=3$, $T_{on\_n}=0.325$, $V_{Ln}=0.4$): (a) in three-dimensional state space; (b) projection onto m_c-j_i state plane; (c) projection onto m_c-j_r state plane.



(a)



(b)

Fig. 2.5. Illustration of the state plane trajectories of: (a) L_i-C_s branch; (b) L_r-C_s branch.

2.5.2. STATE B

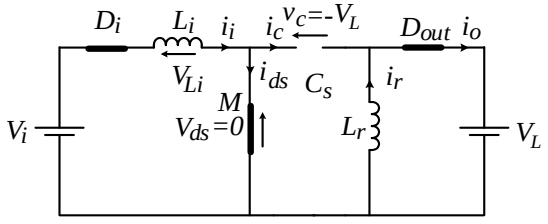


Fig. 2.6. Equivalent circuits of the topological state B.

State B, at t_1-t_2, see Fig. 2.6, commences as diode D_o conducts and establishes a discharge path for L_r to the output, V_L, while clamping C_s to the negative of the output voltage, $-V_L$. Since the switch M is still on, the inductor L_i keeps charging and its current keeps ramping up linearly.

The initial conditions for state B are identical to the final conditions for state A above (2.26), (2.27), (2.28). The normalized solution of state B is obtained referring to the equivalent circuit in Fig. 2.6 and applying the given initial conditions

$$m_{CB}(t) = -V_{Ln} \quad (2.30)$$

$$j_{iB}(t) = \omega_{0i} t \quad (2.31)$$

$$j_{rB}(t) = j_{r1} - \frac{1}{r \cdot I_{base}} \left(\frac{V_L}{L_r} (t - t_1) \right) = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln} \omega_{0r} (t - t_1) \quad (2.32)$$

here, (2.28), (2.10), (2.6), (2.4) and (2.2) were used.

The normalized solution of state B traces a linear segment in both the m_c-j_i and in the m_c-j_r state planes, see Fig. 2.5.

State B is terminated by controller's command at

$$t_2 = T_{on} \quad (2.33)$$

This implies

$$t_B = t_2 - t_1 = T_{on} - t_A \quad (2.34)$$

Thus, at $t=t_2$, state B is concluded with the normalized state variables reaching their final values

$$m_{C2} = m_{CB}(t_2) = -V_{Ln} \quad (2.35)$$

$$j_{i2} = j_{iB}(t_2) = \omega_{0i} t_2 = \omega_{0i} T_{on} = 2\pi T_{on\_n} \quad (2.36)$$

$$j_{r2} = j_{rB}(t_2) = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln} \omega_{0r} t_B \quad (2.37)$$

The above equation may be rewritten as a function of the normalized switch on-time using (2.34), (2.17) and (2.29)

$$j_{r2} = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln} \left[2\pi r T_{on\_n} - \frac{\pi}{2} - sin^{-1} \left(\frac{V_{Ln}}{V_{mn}} \right) \right] \quad (2.38)$$

2.5.3. STATE C

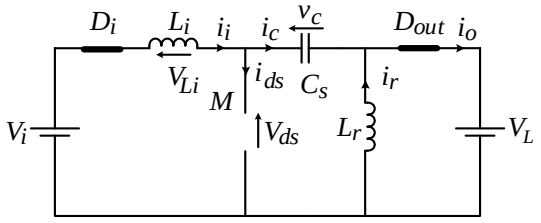


Fig. 2.7. Equivalent circuits of the topological state C.

State C, t_2-t_3, see Fig. 2.7, commences when the switch, M, is turned off, which, thanks to C_s snubbing, occurs at zero voltage, v_{ds}=0. As L_i and C_s resonate, the capacitor C_s is charged to a high voltage while the diode D_o, conducts the resonant current to the output, while L_r is clamped to the output and discharges linearly. State C ends as the inductor L_i is discharged and the diode, D_i, turns off at zero current.

The initial conditions of state C, are identical to the final conditions of state B (2.35), (2.36), (2.37) and can be interpreted as the angle, $\omega_{0i}t_c$, traced in the state-plane, see Fig. 2.5 (a):

$$\omega_{0i}t_C = \pi - \varphi = \pi - \tan^{-1}\left(\frac{j_{i2}}{M_T+V_{Ln}}\right) \qquad (2.39)$$

Solving the equivalent circuit in Fig. 2.7 for the specified initial conditions yields the normalized solution of state C

$$m_{CC}(t) = M_T + R_i\cos(\omega_{0i}(t-t_2) - \omega_{0i}t_C) \qquad (2.40)$$

$$j_{iC}(t) = -R_i\sin(\omega_{0i}(t-t_2) - \omega_{0i}t_C) \qquad (2.41)$$

$$j_{rC}(t) = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln}\omega_{0r}(t-t_1) \qquad (2.42)$$

The solution of state C traces a circular arc in the m_c-j_i state-plane and a sinusoidal arc in the m_c-j_r state plane, see Fig. 2.5. (Note that (2.42) returns a positive result.) The circular arc C in the m_c-j_i state-plane, see Fig. 2.5 (a), is centered at

$$M_T = 1 - V_{Ln} \qquad (2.43)$$

and has the radii R_i

$$R_i = \sqrt{(M_T + V_{Ln})^2 + j_{i2}^2} = \sqrt{1 + (\omega_{0i}T_{on})^2} = \sqrt{1 + \left(2\pi T_{on\_n}\right)^2}$$

(2.44)

Here Fig. 2.5 (b) and (2.36) were used.

Note that (2.42) describes the on-going linear discharge of the current, $i_r(t)$, which started at $t=t_1$, see Fig. 2.2, and, therefore, the expression is identical to (2.32).

State C terminates at $t=t_3$ as the normalized current of inductor L_i falls to zero

$$j_{i3} = j_{iC}(t_3) = 0 \qquad (2.45)$$

The duration of state C can be found from (2.39) as

$$t_C = \frac{\pi-\varphi}{\omega_{0i}} = \frac{1}{\omega_{0i}}[\pi - \tan^{-1}(\omega_{0i}T_{on})] = \frac{1}{\omega_{0i}}\left[\pi - \tan^{-1}\left(2\pi T_{on\_n}\right)\right]$$

(2.46)

Here (2.43) and (2.36) were also used.

Hence

$$t_3 = t_2 + t_C \qquad (2.47)$$

At this instant, the normalized current of inductor L_r falls linearly to

$$j_{r3} = j_{rC}(t_3) = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln}\omega_{0r}(t_3 - t_1) \qquad (2.48)$$

whereas, the normalized capacitor voltage, see Fig. 2.5 (a), gets to its peak value of

$$m_{C3} = m_{CC}(t_3) = M_T + R_i = V_{mn} \qquad (2.49)$$

The normalized peak voltage across the capacitor, V_{mn}, is an important system's parameter, which can now be explicitly quantified using (2.43) and (2.44) as

$$V_{mn} = \frac{V_m}{V_i} = M_T + R_i = 1 - V_{Ln} + \sqrt{1 + (\omega_{0i}T_{on})^2} = 1 - V_{Ln} + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2} \qquad (2.50)$$

This also helps to determine (2.24).

2.5.4. STATE D

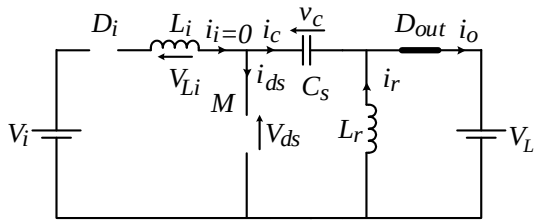


Fig. 2.8. Equivalent circuits of the topological state D.

State D, t_3-t_4, see Fig. 2.8, commences upon the turn off of the diode D_i. The inductor, L_r, continues its linear discharge releasing its stored energy to the output. Meanwhile, the capacitor, C_s, preserves its state.

The normalized solution of state D is

$$m_{CD}(t) = V_{mn} \qquad (2.51)$$

$$j_{iD}(t) = 0 \qquad (2.52)$$

$$j_{rD}(t) = j_{rC}(t) = j_{rB}(t) = \sqrt{V_{mn}^2 - V_{Ln}^2} - V_{Ln}\omega_{0r}(t - t_1) \qquad (2.53)$$

Here, as noted above, the solution (2.53) has the same form as (2.32) and (2.42).

When the inductor, L_r, is totally discharged, and its current drops to zero, the diode, D_o, turns off at zero current and State D is concluded. The linear discharge interval of L_r, t_{BCD}, is the combined duration of states B, C, and D and is given by

$$t_{BCD} = \frac{\sqrt{V_{mn}^2 - V_{Ln}^2}}{V_{Ln}\omega_{0r}} = \frac{1}{\omega_{0r}}\sqrt{\frac{V_{mn}^2}{V_{Ln}^2} - 1} \qquad (2.54)$$

From (2.54) the duration of state D can be obtained as

$$t_{\mathrm{D}} = t_{BCD} - t_B - t_C \qquad (2.55)$$

2.5.5. STATE E

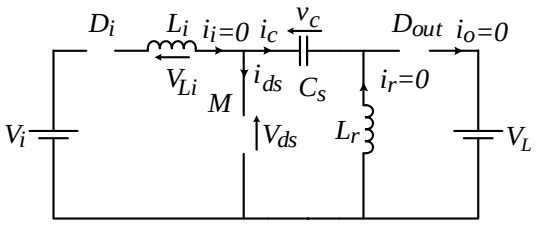


Fig. 2.9. Equivalent circuits of the topological state E.

State E, t_4-T_s, see Fig. 2.9, is the idle state. Here, inductors carry no current and the capacitor, C_s, preserves its state.

$$m_{CE}(t) = V_{mn} \qquad (2.56)$$

$$j_{iE}(t) = 0 \qquad (2.57)$$

$$j_{rE}(t) = 0 \qquad (2.58)$$

State E is terminated when the controller turns on the switch M, and so initiates the next switching cycle.

2.6. KEY PARAMETERS

The state analysis discussed above attained the detailed expressions for all three state variables of the proposed MRCIC. Based on these results key performance characteristics of the MRCIC can be derived as follows.

2.6.1. SWITCH VOLTAGE STRESS

During State D the diode D_o conducts, see Fig. 2.8, and imposes the sum of the peak capacitor voltage, V_m, and the output voltage, V_L, to appear across the switch. Therefore, the normalized peak switch voltage, $V_{dsmn,}$ can be found using as

$$V_{dsmn} = \frac{V_{dsm}}{V_i} = \frac{V_m + V_L}{V_i} = 1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2} \qquad (2.59)$$

The normalized peak switch voltage, $V_{dsmn,}$ (2.59) is plotted in Fig. 2.19 as a function of the normalized on-time, T_{on_n}.

Note that the switch peak voltage is independent of the switching frequency; hence, when the output power of MRCIC is adjusted using switching frequency modulation the switch voltage stress remains constant. This is an operational advantage of the constant T_{on} control strategy.

2.6.2. PEAK INDUCTORS' CURRENTS

Note that the peak normalized maximum capacitor voltage, V_{mn}, and the maximum normalized current through the inductor L_r, J_{rm}, both lay on the circular arc A in Fig. 2.5 (b) and, therefore, are equal to radii R_r and found in

$$J_{rm} = V_{mn} = R_r = 1 - V_{Ln} + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2} = V_{dsmn} - V_{Ln} \qquad (2.60)$$

Also, the normalized peak current through the inductor L_i can be found, see Fig. 2.5(a), as:

$$J_{im} = R_i = \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2} \qquad (2.61)$$

Here (2.44) was used.

2.6.3. SWITCH CURRENT STRESS

The RMS switch current can be found from

$$I_{\mathrm{ds\_rms}} = \sqrt{\frac{1}{\mathrm{T_s}}\left[\int_0^{\mathrm{t_A}} \left(\mathrm{I_{rm}}\sin(\omega_{0r}t) + \mathrm{I_{i2}}\frac{\mathrm{t}}{\mathrm{T_{on}}}\right)^2 \mathrm{dt} + \int_{\mathrm{t_A}}^{\mathrm{T_{on}}} \left(\mathrm{I_{i2}}\frac{\mathrm{t}}{\mathrm{T_{on}}}\right)^2 \mathrm{dt}\right]} \qquad (2.62)$$

The exact solution is quite lengthy and inconvenient for any practical use; therefore, an approximation is attempted by replacing exact t_A time interval with (2.29). The approximated expression for the normalized switch rms current is

$$I_{ds\_rms\_n} = \frac{I_{ds\_rms}}{V_i/Z_{0i}} \approx \sqrt{f_n\left(\frac{r(V_{dsmn}-V_{Ln})^2}{8} + \frac{V_{dsmn}-V_{Ln}}{r\pi} + \frac{4\pi^2 T_{on\_n}{}^3}{3}\right)} \quad (2.63)$$

2.6.4. AVERAGE OUTPUT CURRENT AND POWER

The average output current supplied to the output filter, and the load can be found considering the contribution of the i_i and i_r currents that flow to the output during the appropriate time intervals. Examining the waveform of the output current in Fig. 2.2 (b), and applying the definition of the average current, the general expression for the average output current can be written as follows

$$I_L = \frac{1}{T_s}\int_0^{T_s} i_o(t)dt = \frac{1}{T_s}\left[\int_{t_2}^{t_3} i_i(t)dt + \int_{t_1}^{t_4} i_r(t)dt\right] \quad (2.64)$$

The first integral term in (2.64) can be recognized as the charge acquired by the capacitor during state C, whereas the second integral term is merely the area of a triangle segment in $i_r(t)$ waveform, see Fig. 2.2 (b), therefore

$$I_L = \frac{1}{T_s}\left[C_s(V_m + V_L) + \frac{1}{2}C_s\frac{(V_m^2 - V_L^2)}{V_L}\right] \quad (2.65)$$

In the steady state, the average output power, P_L, per switching cycle, T_s, can be found according to

$$P_L = V_L I_L = \frac{C_s}{T_s}\left[V_L(V_m + V_L) + \frac{(V_m^2 - V_L^2)}{2}\right] = f_s C_s \frac{V_{dsm}^2}{2} = f_s C_s \frac{V_i^2}{2}\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2 \quad (2.66)$$

here, (2.59) was used.

The normalized output power, P_n, can be obtained from (4.33), and using (2.66), (2.59), (2.3), (2.14) and (2.13)

$$P_n = \frac{P_L}{\left(\frac{V_i{}^2}{Z_{0i}}\right)} = f_n \frac{V_{dsmn}^2}{4\pi} = \frac{f_n}{4\pi}\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2 \quad (2.67)$$

Here, an important observation can be made- since the output power is independent of the load, it is clear that the proposed MR CIC has a controlled power source characteristic.

2.6.5. OUTPUT VOLTAGE AND CURRENT

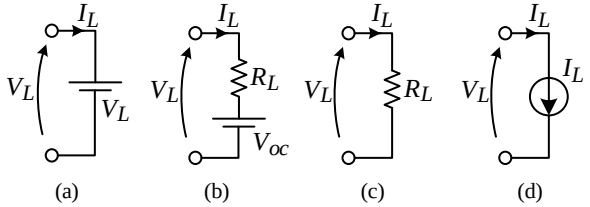


Fig. 2.10. Illustration of different loads: (a) ideal voltage sink, V_L; (b) non-ideal voltage sink; (c) resistive load, R_L; (d) ideal current sink, I_L.

Hitherto, the analysis was performed under the assumption of an ideal voltage sink load, V_L, shown in Fig. 2.10 (a). Accordingly, the response of the output current was found (2.65). This current may be rewritten as a function of output power:

$$I_L = \frac{P_L}{V_L} = f_s C_s \frac{V_{dsm}^2}{2V_L} = f_s C_s \frac{V_i^2}{2V_L}\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2 \tag{2.68}$$

However, other load types can be considered.

In case of a non-ideal voltage sink load, having an open circuit voltage, V_{oc}, and an equivalent series resistance, R_L, see Fig. 2.10 (b), load power is given by

$$P_L = I_L V_L = \left(\frac{V_L - V_{oc}}{R_L}\right) V_L \tag{2.69}$$

Substituting (2.66) for the output power, P_L, and solving for output voltage, V_L, yields:

$$V_L = \frac{V_{oc}}{2} + \frac{1}{2}\sqrt{V_{oc}^2 + 2R_L f_s C_s V_i^2\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2} \tag{2.70}$$

while the output current, I_L, is given by

$$I_L = -\frac{V_{oc}}{2R_L} + \frac{1}{2R_L}\sqrt{V_{oc}^2 + 2R_L f_s C_s V_i^2\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2} \tag{2.71}$$

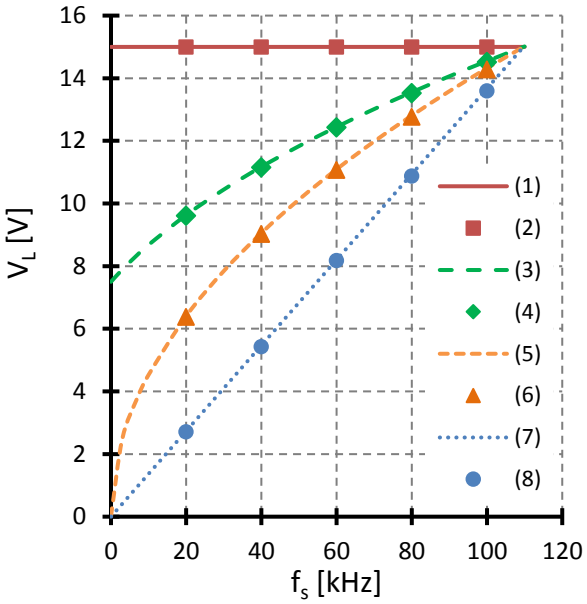
In case of a purely resistive load, R_L, see Fig. 2.10 (c), the dc output voltage of the MRCIC can be found from (2.70) simply by substituting $V_{oc} = 0$ as

$$V_L = \sqrt{P_L R_L} = V_i\sqrt{\frac{1}{2} f_s C_s R_L\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2} \tag{2.72}$$

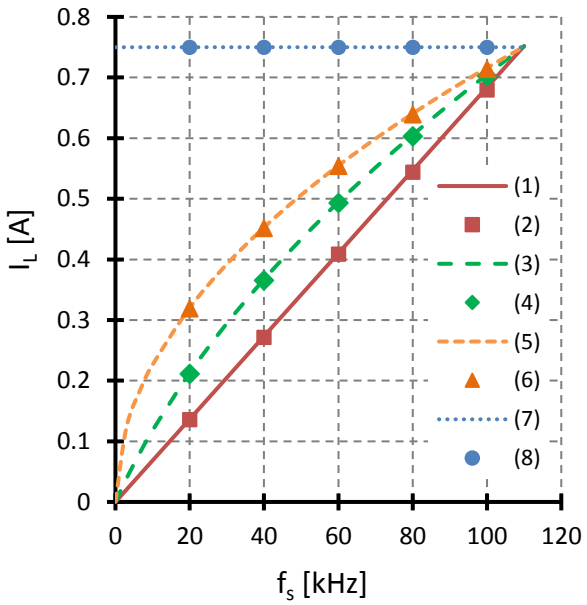
Lastly, in case of a constant current load, I_L, see Fig. 2.10 (d), the output voltage is given by:

$$V_L = \frac{P_L}{I_L} = f_s C_s \frac{V_i^2}{2I_L}\left[1 + \sqrt{1 + \left(2\pi\, T_{on\_n}\right)^2}\right]^2 \tag{2.73}$$

see Fig. 2.11 for comparison of calculated vs. simulated values.



(a)



(b)

Fig. 2.11. Comparison of the calculated vs. the simulated (a) output voltage, V_L, and (b) output current, I_L, as a function of switching frequency, f_s.,Simulation parameters as described in Simulation and Experimental Verification, T_{on}=2 μs. Used legend: odd indexes - calculated values, even indexes - simulated data:
(1),(2) – Ideal voltage sink V_L=15V;
(3),(4) – Non-ideal current sink V_{oc}=7.5V, R_L=10ohm;
(5),(6) – Resistive load, R_L=20ohm;
(7),(8) - Ideal current sink, I_L=0.75A.

2.6.6. OUTPUT VOLTAGE RIPPLE

The output voltage ripple arises due to the difference between the instantaneous and the average output currents $i_o(t)$-I_L, see Fig. 2.12.

$$\Delta V_L = \frac{\Delta Q}{C_L} \tag{2.74}$$

From Fig. 2.12:

$$\Delta Q = I_L T_s - q_x \tag{2.75}$$

Applying geometrical considerations, one can find:

$$q_x = \frac{1}{2} I_1 t_{BCD} \left(1 - \left[\frac{I_1 - I_L}{I_1}\right]^2\right) \tag{2.76}$$

where I_1 is the value of the output current at the vertex point of the triangle, see Fig. 2.12, which can be found from (2.27) as

$$I_1 = j_{r1} I_{base} \tag{2.77}$$

and $I_L = P_L / V_L$ is the average output current.

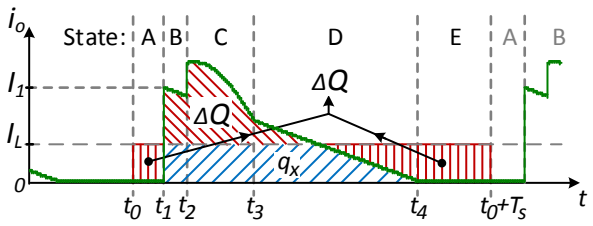


Fig. 2.12. Current differences between average, I_L, and instantaneous current, $i_o(t)$, creating fluctuations of charge, ΔQ, in the output capacitor, C_L .

Substituting (2.76), (2.77), (2.28), (2.10), (2.54), (2.68), and (2.3) into (2.75) yields:

$$\Delta Q = \frac{1}{2} \frac{V_{dsmn}^2}{V_{Ln}} V_i C_s \left(1 - \frac{f_s \sqrt{L_i C_s} \sqrt{(V_{dsmn} - V_{Ln})^2 - V_{Ln}^2}}{r\, V_{Ln}} + \frac{L_i C_s V_{dsmn}^2 f_s^2}{4\, r\, V_{Ln}^2}\right) \tag{2.78}$$

Hence, the output ripple coefficient can be derived combining (2.74) and (2.78)

$$\gamma = \frac{\Delta V_L}{V_L} = \frac{\Delta Q}{C_L V_L} = \frac{1}{2} \frac{V_{dsmn}^2}{V_{Ln}^2} \frac{C_s}{C_L} \left(1 - \frac{f_s \sqrt{L_i C_s} \sqrt{(V_{dsmn} - V_{Ln})^2 - V_{Ln}^2}}{r\, V_{Ln}} + \frac{L_i C_s V_{dsmn}^2 f_s^2}{4\, r\, V_{Ln}^2}\right) \tag{2.79}$$

Regretfully, the exact result (2.79) is unfriendly for engineering applications. Therefore, a simple approximation is attempted.

Considering only the triangular component while neglecting the superimposed quasi-sinusoidal segment of the current $i_o(t)$, see Fig. 2.2 (b), the charge difference can be approximated by $\Delta Q_S \approx \frac{T_S I_L}{2}$. Accordingly, the switching ripple at the output can be estimated by

$$\Delta V_L \approx \frac{\Delta Q_S}{C_L} = \frac{1}{C_L}\frac{1}{2}T_S I_L = \frac{V_L}{2 f_S C_L R_L} \qquad (2.80)$$

The resulting approximate expression for the ripple coefficient is much simplified:

$$\gamma = \frac{\Delta V_L}{V_L} \approx \frac{1}{2 f_S C_L R_L} \qquad (2.81)$$

The comparison of the theoretical and the simulation results is given in Fig. 2.13 below.

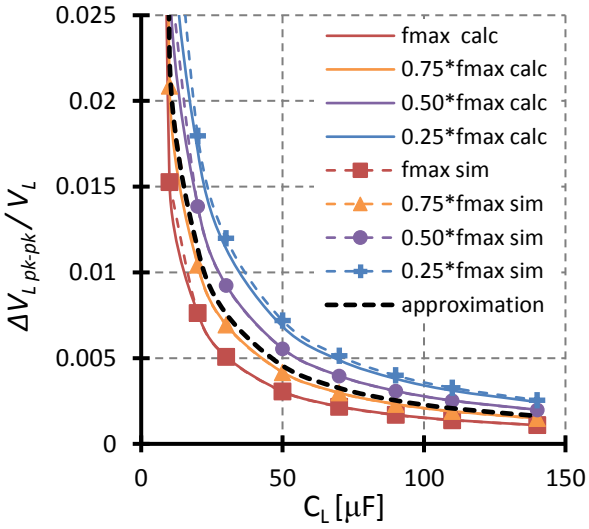


Fig. 2.13. Comparison of the calculated vs. the simulated output ripple as a function of output capacitor value, C_L, for different switching frequencies relative to the maximal switching frequency, f_{s_max}, using an equivalent load resistor R_L=19.24 Ohm@f_{s_max} , f_{s_max}=114 kHz, T_{on}=2 µs. Resistor adjusted accordingly to changes in switching frequency to keep the output voltage constant, V_L=15 V.

2.6.7. MINIMUM SWITCH ON-TIME

For the state C to exist the switch conduction time, T_{on}, should be longer than the duration of state A, see (2.34). And hence the shortest on time, T_{on_min}, can be defined, using (2.29):

$$T_{on\_min} = t_A = \frac{1}{\omega_{0r}}\left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right)\right] \qquad (2.82)$$

Which can be written in the normalized notation using (2.16) and as:

$$T_{on\_\min\_n} = \frac{t_A}{T_{base}} = \frac{1}{2\pi r}\left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{1-V_{Ln}+\sqrt{1+\left(2\pi T_{on\_\min\_n}\right)^2}}\right)\right] \quad (2.83)$$

The recursive equation (2.83) poses some calculation difficulties. Yet, a numerical solution to $T_{on\_\min\_n}(r, V_{Ln})$ can be found and is plotted for selected values of inductors ratios, r^2, as shown in Fig. 2.14.

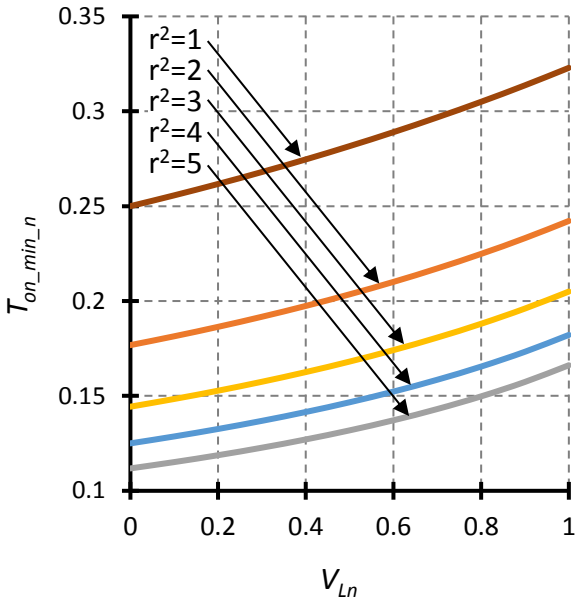


Fig. 2.14 Normalized minimal on-time, $T_{on\_min\_n}$, as a function of the normalized load voltage, V_{Ln}, and selected values of inductors ratio, r^2.

2.6.8. MAXIMUM SWITCHING FREQUENCY

Under the variable frequency constant T_{on} control strategy, the increasing of the switching frequency brings about to shortening of the duration of state E. Nevertheless, due to constant T_{on}, the key parameters and the combined duration of states A, B, C, and D, t_{ABCD}, remains unaltered. Therefore, in order to allow the whole sequence of events to be completed as described the switching period should be longer than a certain minimum value T_{s_min} which equals the combined duration of states, t_{ABCD},

$$T_{s\_min} = t_4 - t_0 = t_{ABCD} = t_A + t_{BCD} = \frac{1}{\omega_{0r}}\left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right) + \sqrt{\frac{V_{mn}^2}{V_{Ln}^2} - 1}\right] \quad (2.84)$$

here (2.29) and (2.54) were used.

This sets an upper limit on the switching frequency, $f_{s\_max} = \frac{1}{T_{s\_min}}$. The resulting normalized highest switching frequency can be obtained from (2.14) using (2.84) and (2.16) as

$$f_{n\_max} = \frac{f_{s\_max}}{f_{os}} = \frac{T_{base}}{T_{s\_min}} = 2\pi r \left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right) + \sqrt{\frac{V_{mn}^2}{V_{Ln}^2} - 1}\right]^{-1} \quad (2.85)$$

Using (2.59) yields:

$$f_{n\_max} = 2\pi r \left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{dsmn} - V_{Ln}}\right) + \sqrt{\frac{V_{dsmn}^2}{V_{Ln}^2} - 2\frac{V_{dsmn}}{V_{Ln}}}\right]^{-1} \quad (2.86)$$

2.6.9. MAXIMUM OUTPUT POWER

As mentioned, the proposed MRCIC behaves as a constant power source with its' output power depending on the normalized switching frequency, f_n, and the switch on time, T_{on_n}. With fixed T_{on_n} and f_n load variations cause changes in the normalized output voltage, V_{Ln}. Therefore, a closed loop control scheme is needed to properly adjust the switching frequency so to keep the output voltage stable against the source and load variations. The controller, however, should not violate f_{n_max} given by (2.86). As a result of the limited switching frequency the available output power, P_{max}, that MRCIC can provide to the load is also limited. The maximum normalized output power can be expressed using (2.67) and (2.86) as

$$P_{n\_max} = f_{n\_max}\frac{V_{dsmn}^2}{4\pi} = \frac{rV_{dsmn}^2}{2}\left[\frac{\pi}{2} + sin^{-1}\left(\frac{V_{Ln}}{V_{dsmn} - V_{Ln}}\right) + \sqrt{\frac{V_{dsmn}^2}{V_{Ln}^2} - 2\frac{V_{dsmn}}{V_{Ln}}}\right]^{-1}$$

(2.87)

which can be explicitly calculated applying (2.59).

2.7. SIMULATION AND EXPERIMENTAL VERIFICATION

2.7.1. SIMULATION RESULTS

The proposed MRCIC topology was first studied by PSIM simulation. The following parameters were used: the input inductance L_i=78 μH; the resonant inductor: L_r=78 μH; isolations capacitors: $2C_S$=8 nF and output voltage, V_L=15 V. The switching frequency was varied up to f_s=120 kHz. This yields the inductors ratio, r^2=1; the normalized output voltage, V_{Ln}=15/48=0.3125, and from Fig. 2.14 the minimal normalized on-time is $T_{on\_min\_n}$=0.27.

Comparison of the normalized switch RMS current, $I_{ds\_rms\_n}$, for different values of T_{on_n} is shown in Fig. 2.15. Here the exact solution of (2.62) and the approximated solution of (2.63) are compared to simulated values. A good fit is observed.

Comparison of simulated vs. calculated normalized peak inductors' currents (2.60), (2.61) is shown in Fig. 2.16. An excellent match is found.

Comparison of the theoretically predicted and simulated normalized maximal switching frequency, f_{n_max}, (2.85) is plotted in Fig. 2.17 as a function of the normalized on-time, T_{on_n}. Excellent fit is evident.

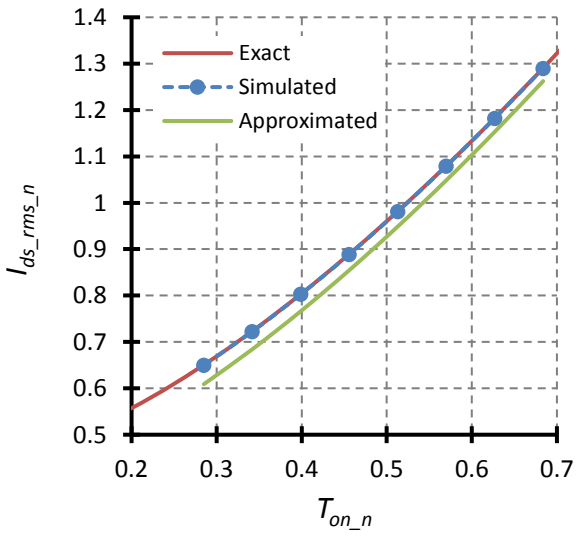


Fig. 2.15. Comparison of normalized switch RMS current, $I_{ds\_rms\_n}$, for different values of T_{on_n}: exact and approximated solutions vs. simulated values.

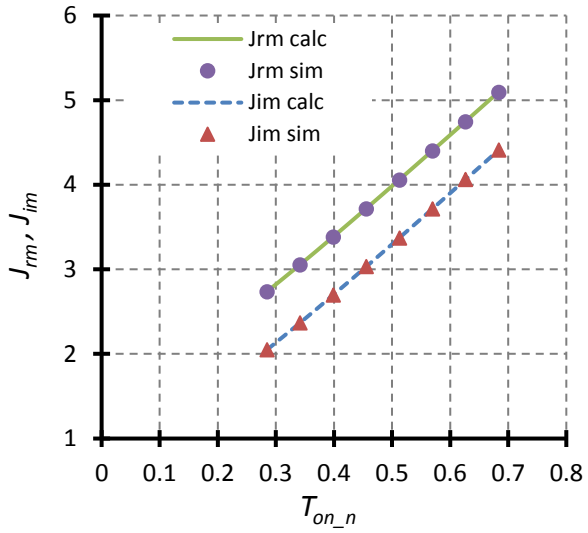


Fig. 2.16. Comparison of simulated vs. calculated normalized peak inductors currents.

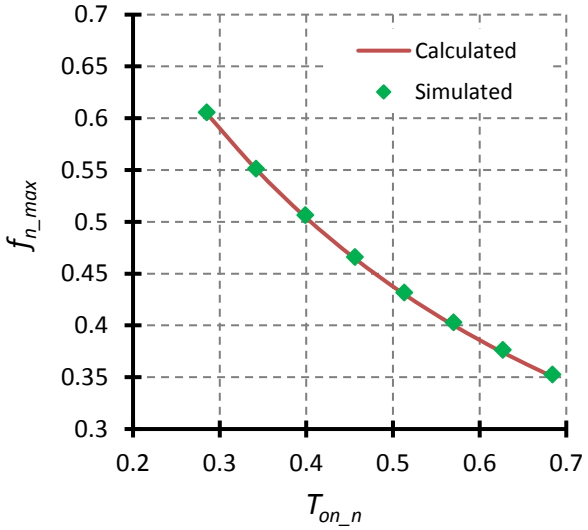


Fig. 2.17. Comparison of simulated vs. calculated normalized maximal switching frequency.

2.7.2. EXPERIMENTAL RESULTS

To further verify the theoretical predictions, a 10 W, 48Vdc input experimental MRCIC prototype in Fig. 2.1 was built and tested. The circuit parameters are summarized in Table 2.1.

Table 2.1. MRCIC Experimental Parameters

Parameter	*Value*
V_i	48 V
Constant Voltage Load, V_L	15 V
$2C_s$	8 nF Kemet 2kV (4.7 nF R73UN14704000J || 3.3 nF R73UN13304000J)
M	Infineon IPP65R225C7XKSA1 (R_{ds}=225mOhm, E_{oss}=2.3µJ @ 400V)
L_i, L_r	78 µHr EPCOS RM10 B65813J0000R049 (N49 ferrite, 38 turns)
D_i, D_o	Cree C3D02060F SiC Diode
C_o	220 µF Electrolytic WIMA EEU-FR1J221L
f_{sm}	115 kHz
T_{on}	2 µs

Key waveforms of the experimental prototype, shown in Fig. 2.18, confirm that zero current switching at turn-on of the switch and zero voltage switching at the turn off of the switch were achieved. Moderate ringing can be noticed in the v_{ds} waveform. Stray inductances of the current probe loop result in current ringing that can be observed in i_o waveform.

Normalized peak switch voltage, V_{dsmn}, is plotted for different values of T_{on_n} in Fig. 2.19. According to Fig. 2.14, for the given $r^2=1$ and $V_{Ln}=15/48=0.3125$ the minimal normalized on-time is $T_{on\_min\_n}=0.27$. Good matching of the experimental and predicted (2.59) results are found.

The input and output power of the proposed MRCIC is shown in Fig. 2.20 (a) in comparison with the theoretical prediction. Good agreement is found. The efficiency plot is given in Fig. 2.20 (b).

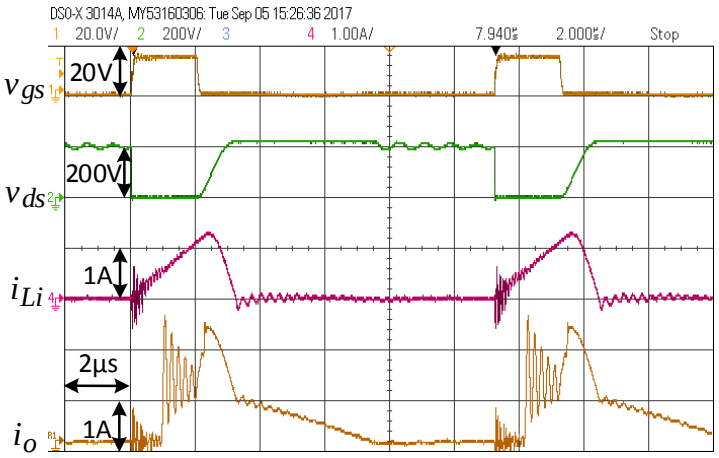


Fig. 2.18. Typical view of the key experimental waveforms of MRCIC, v_{gs}, v_{ds}, i_{Li}, i_o, at the switching frequency scale (Vi=48Vdc, fs=90kHz, Ton=2µs.)

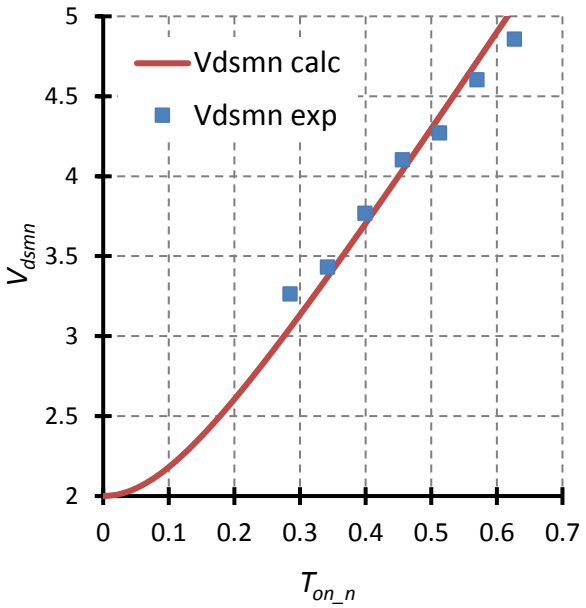
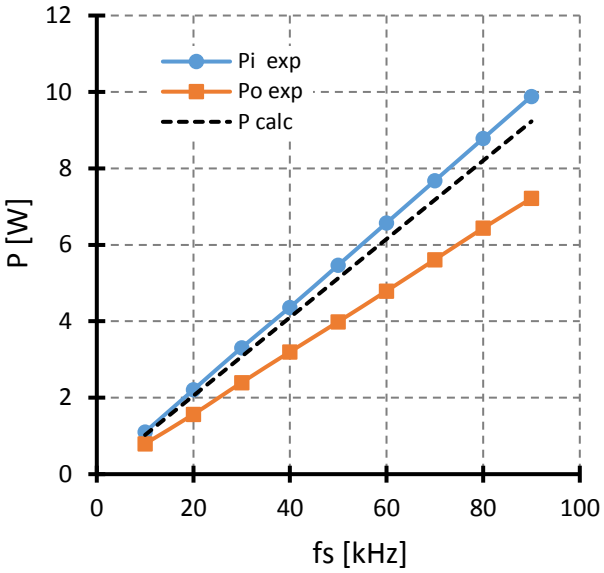
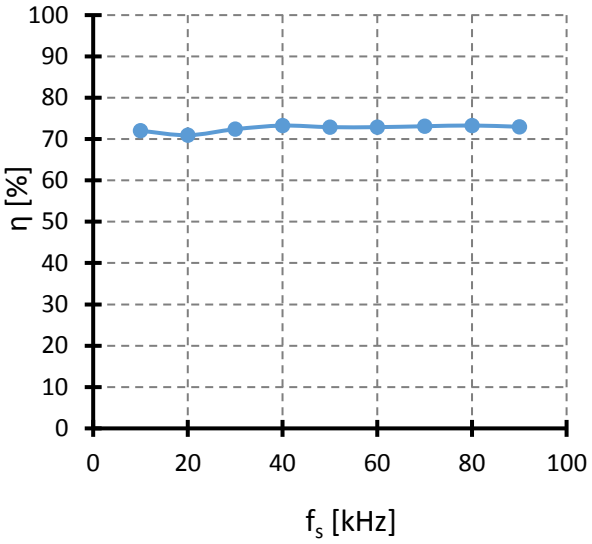


Fig. 2.19. The plot of the normalized peak switch voltage, V_{dsmn}, for different values of T_{on_n}.



(a)



(b)

Fig. 2.20. Experimental results of the MRCIC: (a) comparison of the measured input and output powers vs. the theoretically predicted power; (b) measured efficiency.

CHAPTER 3

MULTI-STRING QUASI-RESONANT LED DRIVER TOPOLOGY

3.1. INTRODUCTION

This chapter proposes a Multi-String (MS) Topology based on previously derived Quasi-Resonant LED Driver (QRLEDD) [37], [38] equal to MRCIC presented in Chapter 2 that is operated from an AC source and used to drive LEDs strings. A method of transition between Single-String (SS) and MS is presented. Applying this method to any topology of the presented converters family [38] from Fig. 1.10 the MS version may be designed. The design procedure for MS QRLEDD is proposed and verified by simulation and experiment on a 3 string version.

The results of this chapter were presented at OPTIM-ACEMP 2017 conference [39] and a more detailed version, "Multi-String Capacitively Isolated Quasi-Resonant LED Driver," submitted for publication considerations.

This work on MS was done before finishing full MRCIC analysis, and the current chapter uses the same base quantities as Reichman, 2015 [37] that differ from ones used in Chapter 2. This does not affect design procedure, and it may be followed step-by-step replacing any normalized quantity by the same quantity from Chapter 2. Due to the differences and missing AC analysis, MRCIC analysis is repeated here shortly using V_{LED} instead of V_L and different base quantities.

3.2. THE PROPOSED TOPOLOGY

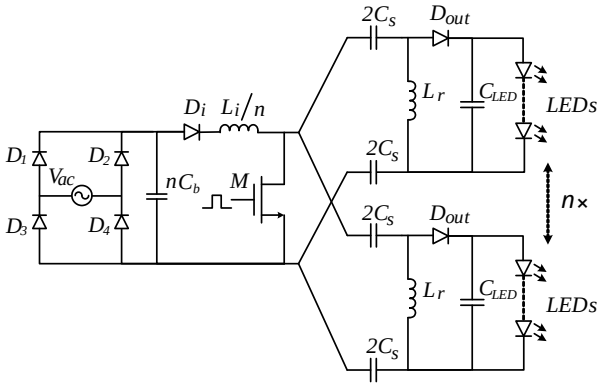


Fig. 3.1. Topology of the proposed MS QR LEDD

The proposed MS QR LEDD is shown in Fig. 3.1. MS QR LEDD has a front semi-stage comprised of a low-frequency bridge rectifier D_1-D_4, with a small high-frequency bypass capacitor, C_b, on its dc port; input inductor, L_i/n; single power switch, M, operated at high frequency; and a fast input diode D_i, in series with L_i to assure unidirectional energy flow. The MS QR LEDD has a number, *n*, of output semi-stages. Each output semi-stage has a pair of small isolating capacitors, $2C_s$; an output inductor L_r; and an output rectifier D_{out}. The LED string is connected across a large filter capacitance, C_{LED}. The output semi-stage of MS QR LEDD provide virtual parallel connection to all the LED strings.

The advantage of the MS QR LEDD topology includes the single ground referenced switch and a gate driver. The switch can operate at high frequency due to zero current turn-on and zero voltage switching turn-off conditions inherently created by the circuit. The isolating capacitors $2C_s$ are also used as a part of the resonant circuit. Capacitive isolation can mitigate the low-frequency mains current to a safe level. With small enough capacitance value, in the range of nanofarads, the current that may flow into a human body in case of a fault can do no harm. However, since the switching frequency is much higher, the same small capacitance can transfer sufficient power to operate low power LED load. These principles are exploited by the proposed MS QR LEDD to offer the capacitive isolation safety feature. With equally sized components of the output semi-stages, MS QR LEDD also has passive balanced power distribution between the LED strings. As discussed below, MS QR LEDD also possesses resistive input port characteristics, which results in low harmonic distortion of the average line current.

3.3. CONVERSION FROM MULTI-STRING TO N-SINGLE-STRINGS

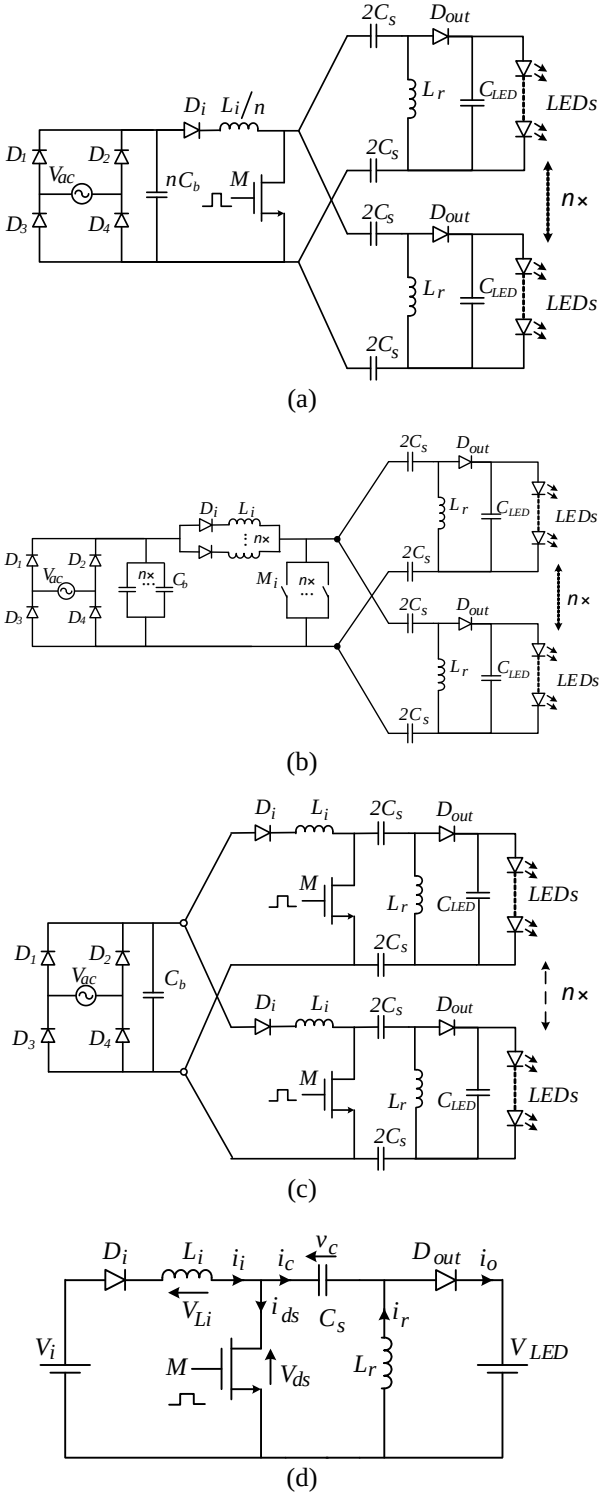


Fig. 3.2. (a) The topology of the proposed MS QR LEDD; (b) the expanded model; (c) equivalent parallel configuration of nx single string drivers; (d) simplified model of a single string driver, QR LEDD.

The n-string MS QR LEDD in Fig. 3.2 (a) can be expanded as shown in Fig. 3.2 (b), and then represented as *n* single-string identical paralleled and synchronized QR LEDD modules connected to the point of common coupling as shown in Fig. 3.2 (c). Note that each single-string QR LEDD module has the input inductor value of the input semi-stage as L_i (n-times larger), whereas the values of the output semi-stage components are equal to those of the original MS QR LEDD. Clearly, the theoretical predictions, derived for the single string QR LEDD, albeit with proper adjustments, are applicable to analysis and design of the original MS QR LEDD topology.

3.4. BASIC ASSUMPTIONS

To further simplify the analysis the following assumptions are adopted: a) the QR LEDD operates in the quasi-steady state equilibrium in the vicinity of a certain value of the input voltage, V_i, which is considered constant within several switching cycles; b) the operating voltage of all the LED strings is assumed equal and constant, thus, neglecting the switching ripple, the LED string and the associated filter capacitance, C_{LED}, can be represented by an equivalent dc voltage sink V_{LED}; c) the equivalent capacitor, C_s, can represent the pair of series blocking capacitors; d) all the semiconductors operate as ideal switches. Applying these considerations to each single string model in Fig. 3.2 (c) yields the yet simplified model of the single string module illustrated in Fig. 3.2 (d).

3.5. QUANTITATIVE ANALYSIS

3.5.1. PRELIMINARY CONSIDERATIONS

Considering the equivalent circuits in Fig. 2.3, Fig. 2.6-Fig. 2.9 and applying state plane approach, see [41] for a brief summary, key parameters of the circuit can be found. For the sake of brevity, some details of derivation are omitted.

During the on interval, $T_{on} = t_2 - t_0 = t_A + t_B$, the input inductor L_i is charged by the input source, V_i, and since the charging commences from zero initial current, the inductor current rises towards

$$I_{i2} = i_i(t_2) = \frac{V_i}{L_i} T_{on} \qquad (3.1)$$

This can be normalized relatively to the base current $I_{base} = V_i / Z_{0i}$, where, $Z_{0i} = \sqrt{\frac{L_i}{C_s}}$ is defined as the characteristic impedance of the L_i-C_s branch, as follows

$$j_{i2} = I_{i2} / \left(\frac{V_i}{Z_{0i}}\right) = \left(\frac{V_i}{L_i} T_{on}\right) / \left(\frac{V_i}{Z_{0i}}\right) = \frac{T_{on}}{\sqrt{L_i C_s}} = \frac{T_{on}}{r\sqrt{L_r C_s}} = \frac{\pi}{2r} T_{on\_n} \qquad (3.2)$$

here, $r^2 = L_i / L_r$ is the inductor ratio, the angular resonant frequency of the L_r-C_s branch is defined as:

$$\omega_{0r} = \frac{1}{\sqrt{L_r C_s}} \qquad (3.3)$$

and the normalized on-time as

$$T_{on\_n} = T_{on} / T_{base} \qquad (3.4)$$

where the base time interval, T_{base}, is defined relatively to a quarter of a resonant cycle of the L_r-C_s branch:

$$T_{base} = \frac{1}{4}\left(\frac{2\pi}{\omega_{0r}}\right) = \frac{\pi}{2}\sqrt{L_r C_s} \qquad (3.5)$$

Examining the waveforms in Fig. 2.6 reveals that at $t=t_2$ the voltage across the capacitor, C_s, is $v_{Cs}(t_2) = -V_{LED}$. This can be normalized relative to the input voltage, V_i

$$m_2 = \frac{v_{Cs}(t_2)}{V_i} = -\frac{V_{LED}}{V_i} = -V_{Ln} \qquad (3.6)$$

where V_{Ln} is defined as the normalized LED string voltage.

During State C, L_i-C_s branch resonates so that at the end of State C the voltage across the capacitor C_s reaches its peak value, $v_{Cs}(t_3) = V_m$. The normalized peak voltage across the capacitor, V_{mn}, can be found

$$V_{mn} = \frac{V_m}{V_i} = M_T + R_i \quad (3.7)$$

Here, the normalized resonant tank voltage, M_T, is

$$M_T = \frac{V_i - V_{LED}}{V_i} \quad (3.8)$$

and the radii, R_i, is:

$$R_i = \sqrt{(M_T + V_{Ln})^2 + j_{i2}^2} \quad (3.9)$$

Combining (3.10) - (3.9) yields the normalized peak capacitor voltage

$$V_{mn} = \frac{V_m}{V_i} = 1 - V_{Ln} + \sqrt{1 + \left(\frac{\pi}{2r} T_{on\_n}\right)^2} \quad (3.10)$$

Introducing the definition of the angular frequency of the L_i-C_s branch:

$$\omega_{0i} = \frac{1}{\sqrt{L_i C_s}} = \frac{1}{r}\omega_{0r} \quad (3.11)$$

the duration of state C can be found as

$$t_C = \frac{1}{\omega_{0i}}\left[\tan^{-1}\left(\left|\frac{M_T + V_{Ln}}{j_{i2}}\right|\right) + \frac{\pi}{2}\right] = \sqrt{L_i C_s}\left[\tan^{-1}\left(\frac{2r}{\pi \cdot T_{on\_n}}\right) + \frac{\pi}{2}\right] \quad (3.12)$$

The peak normalized current through the inductor L_r, j_{rm}, can be found:

$$j_{rm} = I_{rm} / \left(\frac{V_i}{Z_{0r}}\right) = V_{mn} \quad (3.13)$$

where, $Z_{0r} = \sqrt{\frac{L_r}{C_s}}$ is the characteristic impedance of the L_r-C_s branch.

The duration of state A, t_A, is given by

$$t_A = \frac{sin^{-1}\left(\frac{|-V_{Ln}|}{R_r}\right) + \frac{\pi}{2}}{\omega_{0r}} = \frac{1}{\omega_{0r}}\left[sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right) + \frac{\pi}{2}\right] \approx \frac{1}{4}\left(\frac{2\pi}{\omega_{0r}}\right) = T_{base} \quad (3.14)$$

Here, the term $sin^{-1}\left(\frac{V_{Ln}}{V_{mn}}\right)$ can be neglected as the peak capacitor voltage is higher than the LED string voltage, $V_m > V_{LED}$.

The normalized peak output current, j_{r1}, (that appears at the output upon state B commences, $t=t_1$) may be found as:

$$j_{r1} = \sqrt{V_{mn}^2 - V_{Ln}^2} \quad (3.15)$$

and its real value is given by:

$$I_{r1} = \frac{V_i}{Z_{0r}} j_{r1} = \sqrt{\frac{C_s}{L_r} V_i^2 (V_{mn}^2 - V_{Ln}^2)} = \sqrt{\frac{C_s}{L_r}(V_m^2 - V_{LED}^2)} \quad (3.16)$$

The definitions and values found above will be used in the course of the following analysis.

3.5.2. SWITCH VOLTAGE STRESS

During State C the diode D_{out} conducts, see Fig. 2.2 (b), and imposes the *sum* of the peak capacitor voltage, V_m, and the output voltage, V_{LED}, to appear across the switch. Therefore, the normalized peak switch voltage, V_{dsmn}, can be found using (3.10)

$$V_{dsmn} = \frac{V_{dsm}}{V_i} = \frac{V_m + V_{LED}}{V_i} = 1 + \sqrt{1 + \left(\frac{\pi}{2r} T_{on\_n}\right)^2} \tag{3.17}$$

The normalized peak switch voltage (3.17) is plotted in Fig. 3.3 as a function of the normalized on time, T_{on_n}, and the inductor ratio r. Note that the switch peak voltage is independent of the switching frequency. As it is shown in the next section, the output power can be adjusted modulating the switching frequency. Hence, the fact that frequency variations have no effect on switch voltage stress is an operational advantage of the constant T_{on} control strategy.

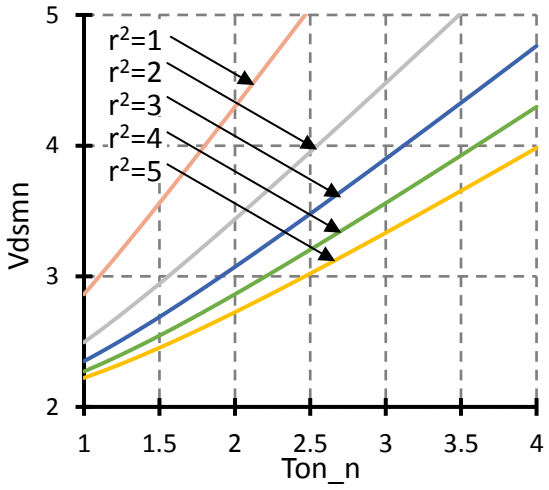


Fig. 3.3. Normalized peak switch voltage, Vdsmn, as function of the normalized on time, Ton_n, and the inductance ratio, r^2.

3.5.3. OUTPUT POWER WITH DC INPUT

The unfiltered output current, supplied to the LED string load $i_o=i_r+i_i$, is illustrated in Fig. 3.4. Two charge components can be identified that contribute to the output energy, E_o. The currents i_i and i_r carry charge quantities q_i and q_r respectively, which contribute to the output energy

$$E_o = E_i + E_r = V_{LED}\,(q_i + q_r) \qquad (3.18)$$

As described above, State A commences when the switch is turned on at the beginning of the switching cycle. Here, L_r-C_s branch resonates, see Fig. 2.3, and the capacitor voltage changes from, $v_c(t_0) = V_m$, to $v_c(t_1) = -V_{LED}$, see Fig. 2.6. The energy, E_r, transferred to the resonant inductor, L_r, is, therefore, the difference

$$E_r = V_{LED} q_r = \frac{1}{2} C_s (V_m^2 - V_{LED}^2) \qquad (3.19)$$

Then, during States C and D, the inductor L_r discharges the acquired energy to the output.

During State C the L_i - C_s branch resonates, and the capacitor voltage is restored from $v_c(t_2) = -V_{LED}$ back to its peak voltage $v_c(t_3) = V_m$, see Fig. 2.7. Since the capacitor C_s is in series with the output circuit, see Fig. 2.8, the charge that flows through C_s is delivered to the load

$$q_i = C_s(V_m + V_{LED}) \qquad (3.20)$$

Therefore, the energy fed to the load is

$$E_i = V_{LED} q_i = C_s V_{LED}(V_m + V_{LED}) \qquad (3.21)$$

The average output power, P_{LED}, per switching cycle, T_s, can now be found considering both energy components E_i and E_r

$$P_{LED} = \frac{E_i+E_r}{T_s} = \frac{C_s}{T_s}\left[V_{LED}(V_m + V_{LED}) + \frac{(V_m^2 - V_{LED}^2)}{2}\right] = \frac{C_s}{T_s}\frac{V_{dsm}^2}{2} = f_s C_s \frac{V_{dsm}^2}{2} \qquad (3.22)$$

where, f_s is the switching frequency. Here (3.18)-(3.21) were used.

The normalized output power, P_n, can be obtained by manipulating (3.22) and using (3.17)

$$P_n = \frac{P_{LED}}{\left(\frac{V_i^2}{Z_{0i}}\right)} = \left(\frac{f_n}{4\pi}\right) V_{dsmn}^2 \qquad (3.23)$$

where, $f_n = \frac{f_s}{f_{0s}}$ is the normalized switching frequency and $f_{0s} = \frac{1}{2\pi\sqrt{L_i C_s}}$ is the resonant frequency of the L_i - C_s branch.

Recall that the analysis above was performed under the assumption that the input voltage to QR LEDD, V_i, is held constant, thus (3.23) is valid for dc operation conditions. When QR LEDD is operated off the utility line, additional considerations apply as described in the next sub-section.

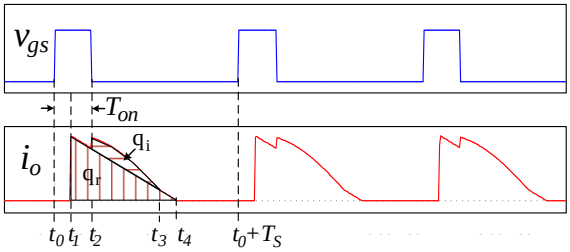
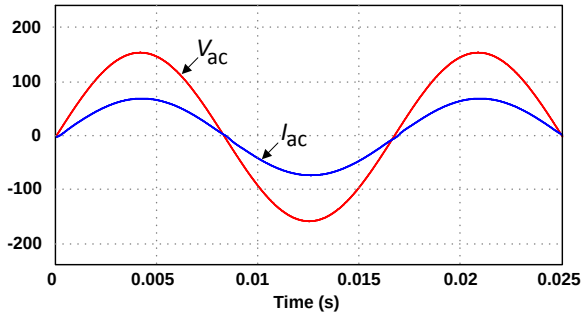
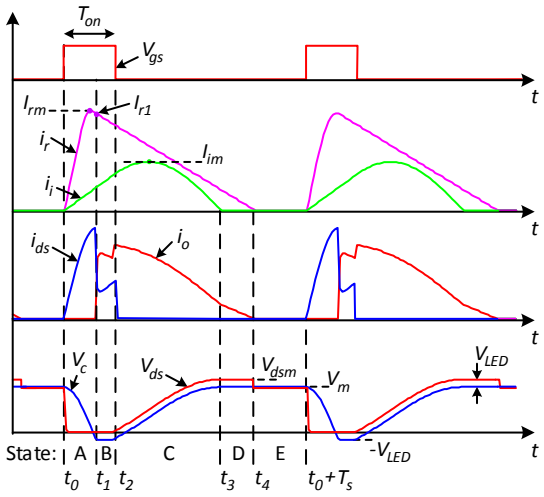


Fig. 3.4. Illustration of the charge components q_i and q_r of the output current, i_o.

3.5.4. OUTPUT POWER WITH AC INPUT



(a)



(b)

Fig. 3.5. Simulated waveforms of the MS QR LEDD: (a) through line period; (b) steady state condition.

The simulated current waveform in Fig. 3.5 (a) suggests that QR LEDD has a resistive input port characteristic. Combining (3.22) and (3.17) the emulated resistance, R_e, at the input port can be found as

$$R_e = \frac{{V_i}^2}{P_{LED}} = \frac{2{V_i}^2}{f_s\, C_s\, V_{dsm}^2} \qquad (3.24)$$

Electronic converter that ideally emulates a resistive load can draw a pure sinusoidal line current and has a peak power, which equals twice the average power, $P_{LED}=2P_{av}$.

Assuming the MS QR LEDD operates in the quasi-steady state regime throughout the line period with fixed T_{on} and f_s the emulated resistance, R_e, (3.24) also holds for AC input. Accordingly, the average power at QR LEDD input port is

$$P_{av} = \frac{1}{2} P_{LED} = \frac{1}{2} \frac{{V_i}^2}{R_e} = \frac{{V_{rms}}^2}{R_e} \qquad (3.25)$$

here V_i stands for the ac line amplitude, and the corresponding line rms voltage is $V_{rms} = \frac{1}{\sqrt{2}} V_i$.

The normalized ac power can be written as follows

$$P_{avn} = \frac{\frac{1}{2} P_{LED}}{\frac{1}{2} {V_i}^2 / Z_{0i}} = \frac{P_{av}}{{V_{rms}}^2 / Z_{0i}} = \left(\frac{f_n}{4\pi}\right) V_{dsmn}^2 = P_n \qquad (3.26)$$

which is identical to (3.23).

3.5.5. DISCONTINUOUS OUTPUT CURRENT MODE BOUNDARY

To attain zero current turn off condition of the output rectifier, D_{out}, calls for maintaining discontinuous output current mode (DCM). This implies the inductor L_r be given sufficient time to complete its charge-discharge cycle. DCM condition sets an upper boundary on the switching frequency, f_{sm}. Accordingly, QR LEDD should be operated in within the specified frequency range, $f_s < f_{sm}$, where DCM prevails. DCM boundary can be found considering the waveform of i_r current, shown in Fig. 3.6. Following considerations apply. The rising edge of the current i_r (here L_r charges) is due to resonant current pulse flowing in the L_r-C_s branch and is about a quarter of a resonant cycle long. To attain soft switching, this current pulse should be allowed to fall to zero before the switch is turned off. Therefore, the minimum switch on time equals the duration of State A, t_A.

The linear fall of i_r (here, L_r discharges) starts with the peak value, $I_{r1} = i_o(t_1)$, which is given by (3.16).

Thus the duration of the linear discharge interval, t_{BCD}, which is the combined duration of States B, C, and D, is:

$$t_{BCD} = t_4 - t_1 = \frac{L_r}{V_{LED}} I_{r1} = \frac{L_r}{V_{LED}} \sqrt{\frac{C_s}{L_r}(V_m^2 - V_{LED}^2)} = \sqrt{C_s L_r} \sqrt{\left(\frac{V_{dsm}}{V_{LED}} - 1\right)^2 - 1} \qquad (3.27)$$

Combining (3.14) and (3.27) the maximum allowable switching frequency, f_{sm}, needed to maintain the DCM operation of the output semi-stage can be derived,

$$f_{sm} = \frac{1}{t_A + t_{BCD}} = \frac{1}{\sqrt{C_s L_r}\left[\frac{\pi}{2} + \sqrt{\left(\frac{V_{dsm}}{V_{LED}} - 1\right)^2 - 1}\right]}. \qquad (3.28)$$

Normalizing it yields:

$$f_{nm} = \frac{f_{sm}}{f_{oi}} = \frac{2\pi r}{\left[\frac{\pi}{2} + \sqrt{\left(\frac{V_{dsmn}}{V_{Ln}} - 1\right)^2 - 1}\right]} = \frac{2\pi r}{\frac{\pi}{2} + \frac{1}{V_{Ln}}\sqrt{\left(\sqrt{1 + \left(\frac{\pi}{2r} T_{on\_n}\right)^2} + 1 - V_{Ln}\right)^2 - V_{Ln}^2}} \quad (3.29)$$

here, V_{dsmn}, V_{Ln}, r, and f_{oi} are as defined above.

Examining (3.29) it is evident that the normalized maximum frequency depends on the inductors ratio, r, the normalized switch on-time, T_{on_n}, and the normalized LED string voltage, V_{Ln} , (3.6).

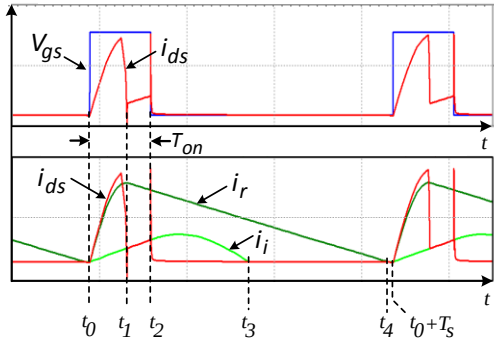


Fig. 3.6. Illustration of the key variables at the DCM-CCM operation mode boundary of the output semi-stage.

3.5.6. PRINCIPAL MODE BOUNDARY

In the preferred mode of operation, the input inductor, L_i, gets discharged before the output inductor, L_r does, see Fig. 3.5 (b) or Fig. 3.6, and allows for state D to occur. The duration of state D, t_4-t_3, is a function of the input voltage. At a certain value of the input voltage, V_{iB}, both inductors complete their discharge exactly at the same instant. Here, t_3=t_4, which means that state D vanishes and the circuit undergoes operational mode change.

The conduction interval, t_3-t_0, of the input inductor current can be expressed as:

$$t_3 - t_0 = T_{on} + t_C \quad (3.30)$$

while the conduction interval, t_4-t_0, of the resonant inductor current can be written as:

$$t_4 - t_0 = t_A + t_{BCD} \quad (3.31)$$

At the mode boundary both intervals (3.30), (3.31) are equal and in normalized notation are given by:

$$T_{on\_n} + t_{Cn} = 1 + \frac{2}{\pi}\sqrt{\left(\frac{V_{dsmn}}{V_{LnB}} - 1\right)^2 - 1} \quad (3.32)$$

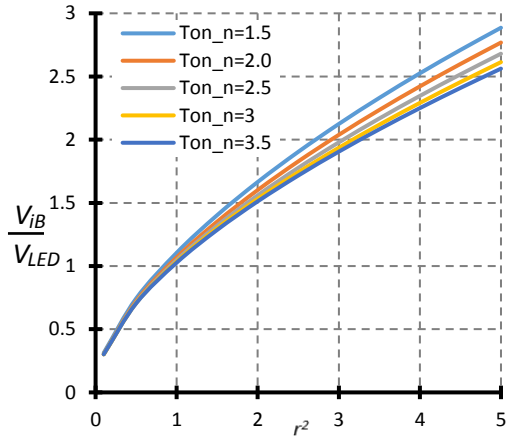
Here (3.4), (3.14) and (3.27) were used and V_{LnB} is defined as

$$V_{LnB} = \frac{V_{LED}}{V_{iB}} \qquad (3.33)$$

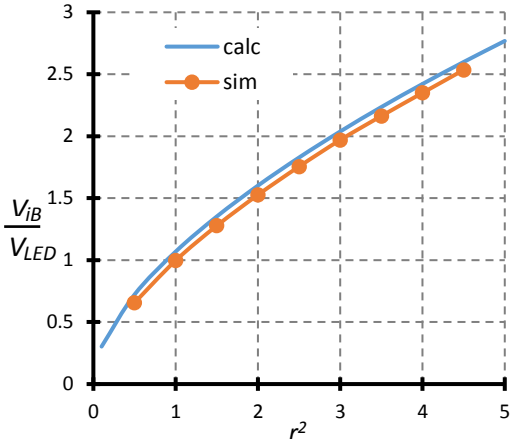
Equation (3.32) can be solved numerically.

The solution is plotted in Fig. 3.7 (a) and illustrates the ratio of the input voltage at the mode boundary to the LED string voltage. According to Fig. 3.7, V_{LnB} strongly depends on the inductors ratio, r^2, and only marginally on T_{on_n}. Theoretical prediction (3.32) was verified by simulation and plotted in Fig. 3.7 (b).

The real value of the input voltage on the onset of the mode change, V_{iB}, can be estimated using the values of V_{LnB} read from the plot and using (3.33). The preferred mode of operation prevails at higher voltage $V_i > V_{iB}$. Therefore, it is desirable to design the mode boundary, V_{iB}, as low as possible.



(a)



(b)

Fig. 3.7. (a) Mode boundary as a function of the LED string voltage, VLED, the inductors ratio, r^2, and the normalized switch on time T_{on_n}; (b) comparison of the predicted vs. simulated mode boundary ratio (for T_{on_n}=2).

3.6. DESIGN CONSIDERATIONS

The design objectives of MS QR LEDD are to establish the required set of hardware parameters L_i, L_r, C_s; the required controller switching frequency, f_s, and on time, T_{on}. Given are the MS QR LEDD specifications of a number of strings, n; AC line voltage, V_{rms}; LED string voltage, V_{LED}, and rated string average power, P_{AVs} (all strings assumed equal).

One possible design approach unfolds as follows.

3.6.1. THE DESIGN EXAMPLE

The objective is designing a three-string MS QR LEDD to operate from V_{rms}=110 V line. Each LED string is specified for the nominal power of P_{AVs}=20 W at V_{LED}=30 V.

a) The inductors ratio, r^2, can be found using Fig. 3.7 so to sustain the desired operational mode starting with a relatively low input voltage, V_{iB}. Recall that L_i/n is the input inductor value, see Fig. 3.2 (a), hence, setting r^2=n, where n is the number of strings, results in equal inductor design $L_r = \frac{L_i}{r^2} = \frac{L_i}{n}$.

- For the given specs r^2=n=3, which yields $L_r = L_i/3$. According to Fig. 3.7, with r^2=3 the input voltage at the onset of the primary operational mode is $V_{iB} \approx 2V_{LED} = 60V$. Hence, for about $\frac{7}{9}\pi$ of each half cycle MS QR LEDD will operate in the primary mode, which is satisfactory.

b) Choose an acceptable peak switch voltage, V_{dsm}, for the given application and calculate its normalized value at the peak of the line $V_{dsmn} = \frac{V_{dsm}}{\sqrt{2}V_{rms}}$. Generally, V_{dsmn} =2.5 seems like an acceptable choice.

- With V_{dsmn} =2.5 the given specs yield an approximate value of V_{dsm}=390V.

c) Using (3.22) and (3.25) and the selected value of V_{dsm}, the product $f_s C_s = \frac{4P_{ACs}}{V_{dsm}^2}$ can be found. Choose a standard value of C_s and find the corresponding switching frequency f_s. Note that to provide the desired capacitive isolation safety feature C_s should be in the range of a few *nF*.

- For this example $f_s C_s = 525.97\,[\mu F] \cdot [\,Hz]$. The capacitors were selected as $2C_s$=4.7||3.3=8nF, (C_s=4nF), thus, the switching frequency of f_s=131.5 kHz is required.

d) The normalized on time can be found from (3.17) as $T_{on\_n} = \frac{2r}{\pi}\sqrt{(V_{dsmn} - 1)^2 - 1}$. Normal operation requires $T_{on\_n} > 1$, therefore, some iteration of r or V_{dsm} can be attempted to attain the desired condition. Alternatively, Fig. 3.3 can be used to obtain an approximate solution.

- Here, the given and the chosen above parameters yield the normalized switch on time: $T_{on\_n} = 1.243$.

e) From (3.29), the maximum normalized switching frequency can be found as $f_{nm} = \frac{2\pi r}{\left[\frac{\pi}{2} + \sqrt{\left(\frac{V_{dsm}}{V_{LED}} - 1\right)^2 - 1}\right]}$.

- In this example, the normalized switching frequency is f_{nm}=0.8044.

f) The input inductor value can be found according to $\frac{L_i}{n} = \frac{1}{nC_s}\left(\frac{1}{2\pi}\frac{f_{nm}}{f_s}\right)^2$

- Here, the calculation results in $L_i/n = 79.0\mu$H.

g) Then, output inductor can be obtained from $L_r = L_i/r^2$.

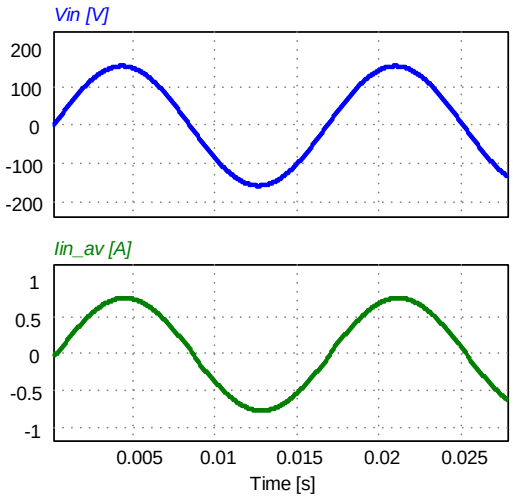
- Whence, $L_r = 79.0\mu H$.

h) Lastly, the required on-time can be found using (3.5) as $T_{on} = T_{on\_n}\frac{\pi}{2}\sqrt{L_r C_s}$.

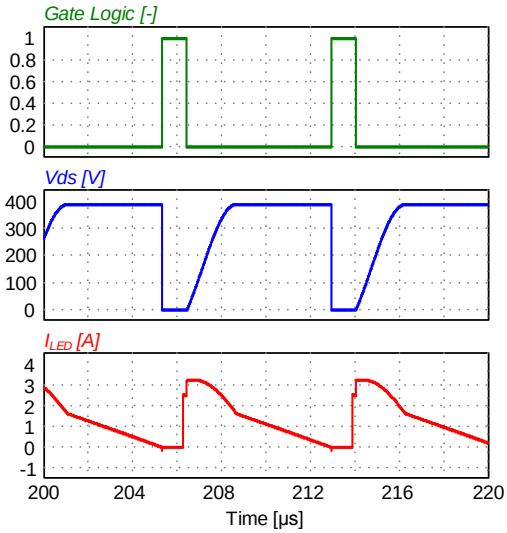
- The required switch on time is found as $T_{on} = 1.10\mu s$.

3.7. DESIGN VERIFICATION

To confirm the design PSIM simulation program was used. The key simulated waveforms of the MS QR LEDD design example are shown in Fig. 3.8. As expected at the peak of the line voltage MS QR LEDD develops peak power and approaches the ZCS boundary of the output rectifier, see Fig. 3.8 (b). The simulated peak switch voltage at the peak of the line is V_{dsm} =389.3 V, matching the expected value of V_{dsm} =390V. The simulated average power throughout the line cycle was P_{av}=59.44W while expected value 3x20W=60W. The simulation results closely match the design objectives and verify the theory and the proposed design approach.



(a)



(b)

Fig. 3.8. Simulated waveforms of the Constant Ton Controlled MS QR LEDD design example. On the line frequency scale: line voltage, V_{ac}, and average line current, I_{ac}, (a); on the switching frequency scale: switch gating signal, V_{gs}, switch voltage, V_{ds} and the output current, i_o (b).

3.8. EXPERIMENTAL RESULTS

Table 3.1. MS QRLEDD Experimental Parameters

Parameter	*Value*
V_i	155 Vdc / 110 Vac 60Hz
n	3 strings
V_{LED}	3x COB 31 V @ 1.6 A
$2C_s$	6x 8 nF Kemet 2kV (4.7 nF R73UN14704000J || 3.3 nF R73UN13304000J)
M	Infineon IPP65R225C7XKSA1 (R_{ds}=225mOhm, E_{oss}=2.3µJ @ 400V)
$\frac{L_i}{n}$, L_{r1}, L_{r2}, L_{r3}	78 µHr EPCOS RM10 B65813J0000R049 (N49 ferrite, 38 turns)
D_i	Cree C3D02060F SiC Diode
D_{o1}, D_{o2}, D_{o3}	CMR5H-06 TR13
C_{o1}, C_{o2}, C_{o3}	220 µF Electrolytic WIMA EEU-FR1J221L
f_{sm}	131.5 kHz
T_{on}	1.1 µs

Experimental MS QR LEDD was build and tested. The parameters of the experimental prototype were (as derived above) according to Table 3.1.

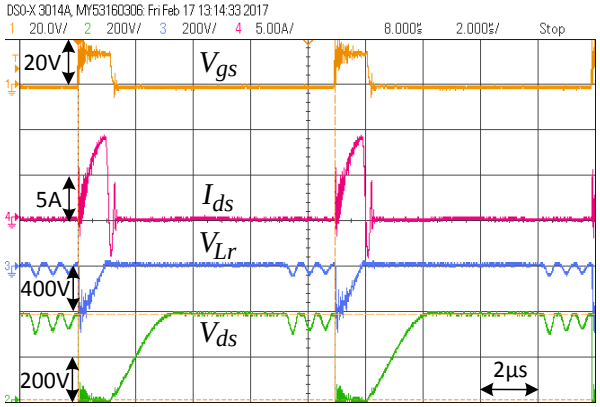
Measured waveforms of the MS QR LEDD on the switching frequency scale are illustrated in Fig. 3.9. The waveforms are in according to the predicted by simulation, see Fig. 3.8.

Comparison of the measured input and output powers vs. the theoretically predicted power and the measured efficiency of MS QR LEDD are plotted in Fig. 3.10. As shown in Fig. 3.11 MS QR LEDD provided excellent power balance in between the LED strings. As mentioned, this result was achieved with no active control.

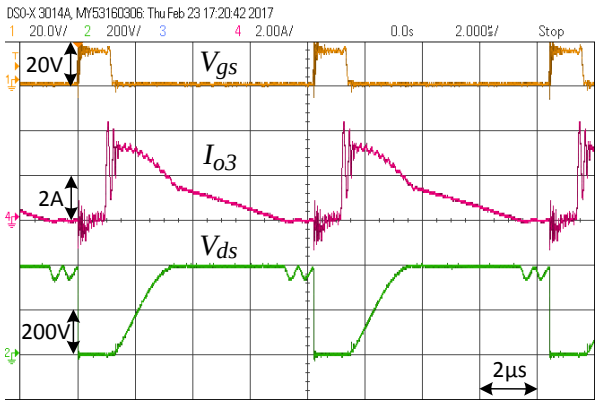
Measured ac line voltage v_{ac} and the average ac line current, i_{ac}, at different power levels (as measured at switching frequencies of 120 kHz, 60 kHz, and 20 kHz) are presented in Fig. 3.12. As could be seen, the average line current is of an excellent quality at full power, however, deteriorating at light load. The measured power factor (PF) and the total harmonic distortion (THD) are presented in Fig. 3.13. Measured THD varied in the 2-18% range.

Fig. 3.14 illustrates the comparison of the theoretically predicted and measured emulated resistance of the MS QR LEDD. The results stand in good agreement.

Losses of the MS QR LEDD were studied by simulation. Simulated loss breakdown as a function of circuit parameter variations is illustrated in Fig. 3.16. Three major factors that have the most detrimental effect on efficiency were the output rectifier on voltage and the diode parasitic capacitance and the switch on resistance.

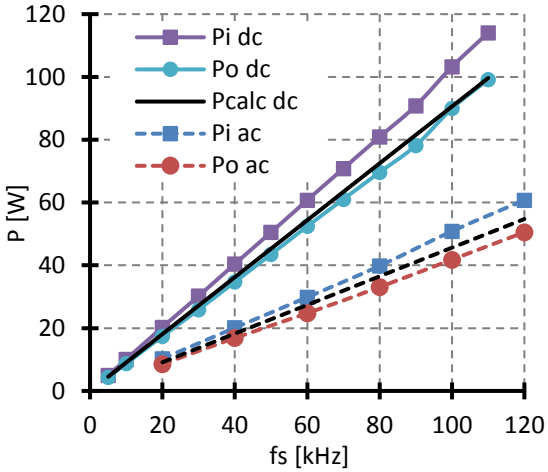


(a)

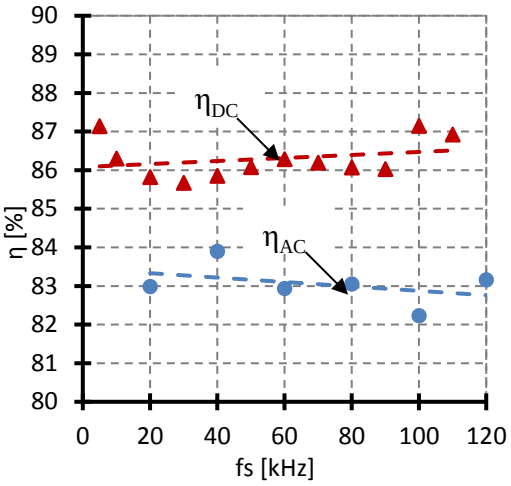


(b)

Fig. 3.9. Experimental results of the MS QR LEDD : typical view of the key waveforms at the switching frequency scale @ Vi=155Vdc: (a) v_{gs}, i_{ds}, v_{Lr}, v_{ds}; (b) v_{gs}, i_o, v_{ds}.



(a)



(b)

Fig. 3.10. Experimental results of the MS QR LEDD : (a) comparison of the measured input and output powers vs. the theoretically predicted power; (b) measured efficiency.

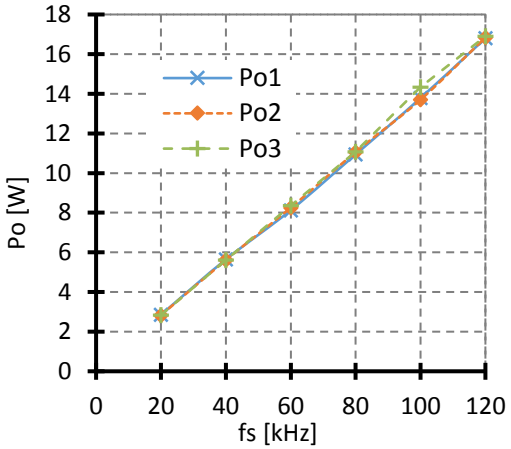


Fig. 3.11. Experimental results of the MS QR LEDD : power balance in between the LED strings at ac input.

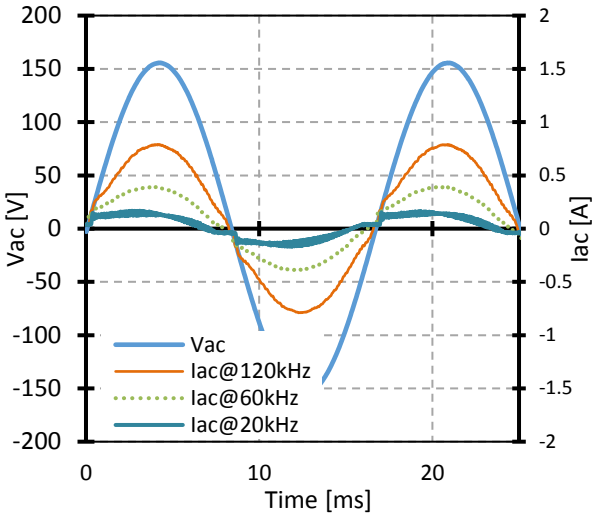


Fig. 3.12. Measured the ac line voltage v_{ac} and the average ac line current, i_{ac}, at different power levels (switching frequencies).

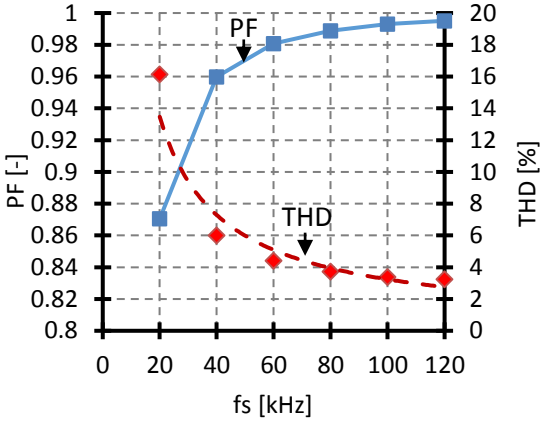


Fig. 3.13. Experimental results of the MS QR LEDD : (a) the power factor (PF) and the total harmonic distortion (THD) performance indices at different power levels.

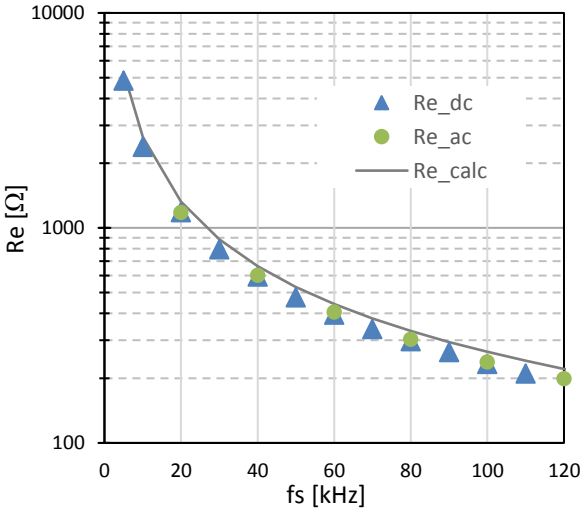


Fig. 3.14. Comparison of the measured vs. calculated equivalent input resistance, R_e, for ac and dc inputs.

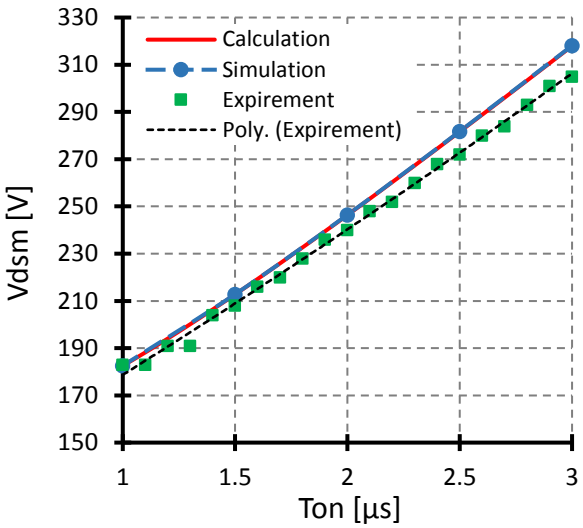


Fig. 3.15. Comparison of the measured vs. calculated vs. simulated peak switch voltage, V_{dsm}.

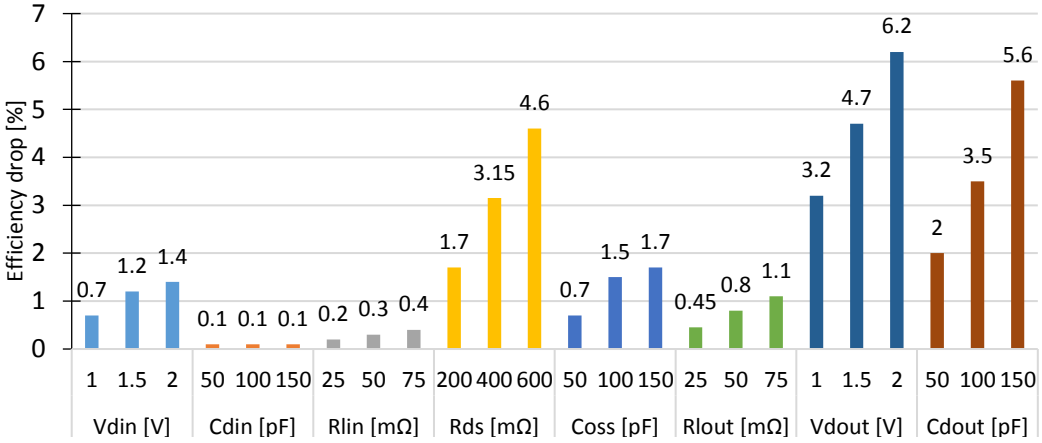


Fig. 3.16. Impact of circuit parameters on MS QR LEDD efficiency (simulated).

CHAPTER 4

CURRENT DOUBLER AND COUPLED CURRENT DOUBLER QUASI-RESONANT LED DRIVER TOPOLOGIES

4.1. INTRODUCTION

This chapter based on results presented at the European Conference on Power Electronics and Applications 2016 (EPE'16) [40]. Paragraph "Parallel and Series Inductors Connection" proofs that the analysis also applies to CD version of CCD topology that was presented.

4.2. TOPOLOGIES OVERVIEW

The proposed topologies of the capacitively isolated Quasi-Resonant LED Driver with Current Doubler Rectifier (CD) and Coupled Current Doubler Rectifier (CCD-QRLEDD) are shown in Fig. 4.1. The proposed topologies are comprised of a low-frequency bridge rectifier D_1-D_4, with a small high-frequency bypass capacitor, C_b, on its dc port. The input inductor, L_i, is switched by the switch, M_1, to shape and control the magnitude of the input current. Fast input diode D_i, in series with L_i, assures unidirectional energy flow. The capacitive isolation barrier is created by a pair of small series blocking capacitors, $2C_s$. The diodes D_{o1} and D_{o2} serve as output rectifier. The LED string load is connected across the filter capacitance, C_{LED}.

The proposed circuit was derived from earlier version MRCIC by modifying the output filter. The shortcomings of the simple inductive filter, used in the earlier counterpart, are relatively high switch rms current and long discharge time to output. The later feature limits the switching frequency. Due to the higher input impedance of the coupled inductor filter lower switch current can be attained. Whereas the discharge towards the LED load is faster

and as a result higher switching frequency can be attained. Hence, compared to the earlier version CD and CCD -QRLEDD are expected to provide better performance indexes.

The merits of CD and CCD-QRLEDD are a single ground referenced switch and gate driver. The switch can operate at high frequency due to zero current turn-on and zero voltage turn-off switching conditions inherently created by the circuit. Hence, CCD-QRLEDD operates in a quasi-resonant mode with discontinuous input and the output currents. Isolating capacitors are also used as a part of the resonant circuit. Another prominent feature of the CCD-QRLEDD is its resistive input port characteristics, which stems from discontinuous current mode operation of the input inductor.

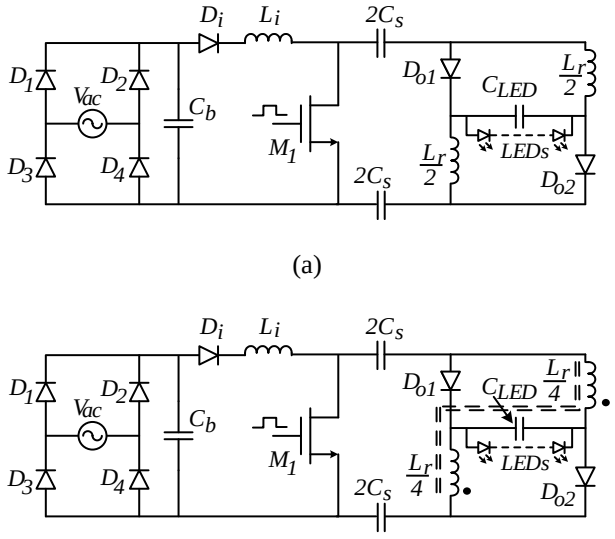
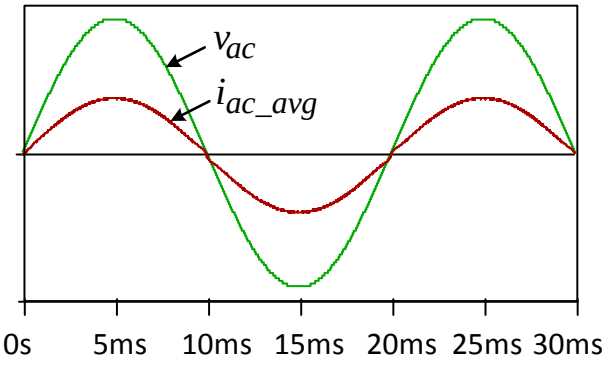
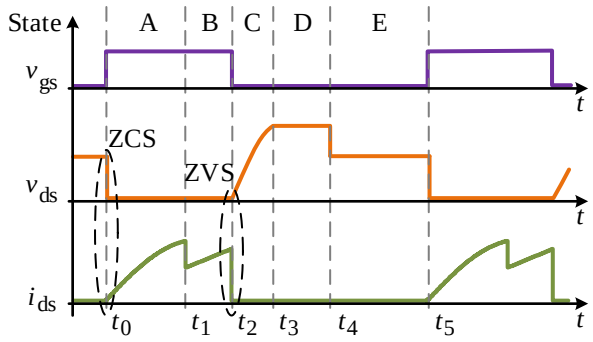


Fig. 4.1. Proposed topologies of Capacitively Isolated Quasi-Resonant LED Driver with: (a) Current Doubler (CD) Rectifier; (b) Coupled Current Doubler (CCD) Rectifier.

Typical waveforms of the proposed topologies on the line frequency and on the switching frequency scale are illustrated in Fig. 4.2 . The average line current waveform, iac, shown in Fig. 4.2 (a) appears as a near sinusoidal signal, which manifests that the CD/CCD-QRLEDD possesses inherently high power factor and low harmonic content. Examining the switch waveforms in Fig. 4.2 (b) reveals favorable zero current (ZC) turn on and zero voltage (ZV) turn off switching of the MOSFET switch, which are a prerequisite to attain high efficiency at high frequency.



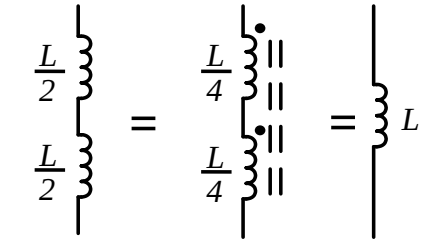
(a)



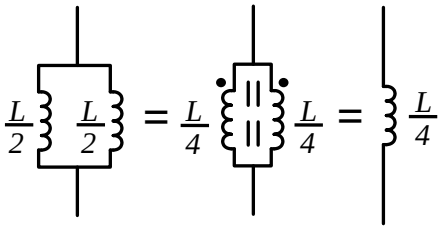
(b)

Fig. 4.2. Simulated waveforms of the proposed CCD-QRLEDD: (a) on the line cycle scale: outer- line voltage, vac, inner- average line current, iac_avg; (b) on the switching cycle scale: top- gating voltage vgs; middle- switch voltage, vds; bottom- switch current, ids.

4.3. PARALLEL AND SERIES INDUCTORS CONNECTION



(a)



(b)

Fig. 4.3. Rules of equivalence of inductors and coupled inductors connections: (a) series connections; (b) parallel connections.

4.3.1. SERIES CONNECTIONS

Looking on Fig. 4.3 (a) it is evident that the series connection shares the same current, while overall voltage is the sum of each inductor's voltages:

$$I_1 = I_2 = I_{eq} \tag{4.1}$$

$$V = V_1 + V_2 \tag{4.2}$$

Using inductor's voltage-current relation we get equivalent value for a single inductor, assuming that L_1=L_2=L:

$$\frac{dI_1}{dt} = \frac{dI_2}{dt} = \frac{dI_{eq}}{dt} \tag{4.3}$$

$$L_{eq}\frac{dI_{eq}}{dt} = L_1\frac{dI_1}{dt} + L_2\frac{dI_2}{dt} \tag{4.4}$$

$$L_{eq} = L_1 + L_2 = 2L \tag{4.5}$$

For coupled inductors, we have an addition of mutual inductance, *M*, which in the case of perfectly coupled (k=1) equal inductors is

$$M = k\sqrt{L_1 L_2} = L \tag{4.6}$$

and hence:

$$L_{eq}\frac{dI_{eq}}{dt} = L_1\frac{dI_1}{dt} + L_2\frac{dI_2}{dt} + M\frac{dI_1}{dt} + \mathrm{M}\frac{dI_2}{dt} \quad (4.7)$$

$$L_{eq} = 4L \quad (4.8)$$

proving relation in Fig. 4.3 (a).

4.3.2. PARALLEL CONNECTIONS

Looking at Fig. 4.3 (b) it is evident that parallel connection shares the same voltage, while the overall current is a sum of each inductor's currents:

$$I_{eq} = I_1 + I_2 \quad (4.9)$$

$$V \ = V_1 = V_2 \quad (4.10)$$

Using inductor's voltage-current relation, we get equivalent value for a single inductor, assuming that L_1=L_2=L:

$$\frac{dI_{eq}}{dt} = \frac{dI_1}{dt} + \frac{dI_2}{dt} \quad (4.11)$$

$$V = L_{eq}\frac{dI_{eq}}{dt} = L_1\frac{dI_1}{dt} = L_2\frac{dI_2}{dt} \quad (4.12)$$

$$\frac{\mathrm{V}}{L_{eq}} = \frac{\mathrm{V}}{L_1} + \frac{\mathrm{V}}{L_2} \quad (4.13)$$

$$L_{eq} = \frac{1}{2}L \quad (4.14)$$

For coupled inductors, we have addition of mutual inductance, *M*, which in case of perfectly coupled (k=1) equal inductors is

$$M = k\sqrt{L_1L_2} = L \quad (4.15)$$

and hence:

$$V = L_{eq}\frac{dI_{eq}}{dt} = L_1\frac{dI_1}{dt} + \mathrm{M}\frac{dI_2}{dt} = L_2\frac{dI_2}{dt} + M\frac{dI_1}{dt} \quad (4.16)$$

$$L_{eq}\left(\frac{dI_1}{dt} + \frac{dI_2}{dt}\right) = L\left(\frac{dI_1}{dt} + \frac{dI_2}{dt}\right) \quad (4.17)$$

$$L_{eq} = L \quad (4.18)$$

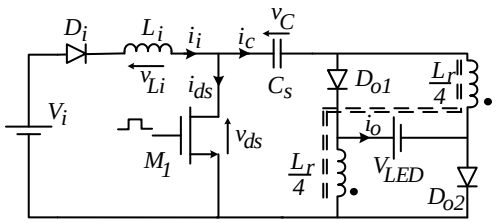
proving relation in Fig. 4.3 (b).

Applying these rules on CD and CCD QRLEDD topologies gives exactly same states circuits in the following analysis, and hence the analysis that was done for CCD is valid also for CD version.

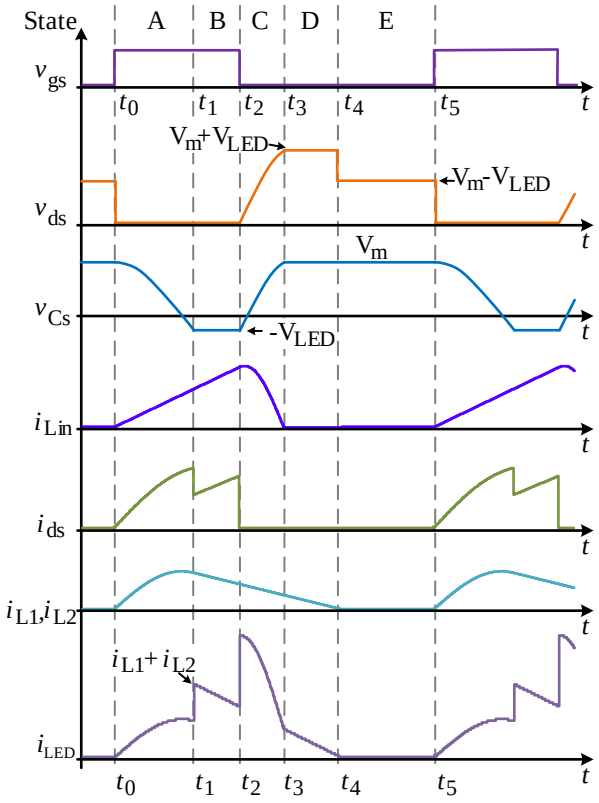
4.4. STATES ANALYSIS

4.4.1. BASIC ASSUMPTIONS

To simplify the analysis the following assumptions are adopted: a) the CCD-QRLEDD operates in the quasi-steady state equilibrium in the vicinity of a certain value of the input voltage, V_i, which is considered constant; b) the operating voltage of the LED string, V_{LED}, is constant, thus, the LED string and the associated filter capacitance, C_{LED}, can be represented by an equivalent dc voltage source; c) the equivalent capacitor, C_s, represents the pair of series blocking capacitors; d) all the semiconductors operate as ideal switches. The resulting model is shown in Fig. 4.4 (a). The detailed steady-state waveforms are presented in Fig. 4.4 (b).



(a)



(b)

Fig. 4.4. The proposed CD/CCD-QRLEDD in the steady state: (a) simplified equivalent circuit; (b) simulated waveforms.

Analysis of the CCD-QRLEDD waveforms in Fig. 4.4 (b) reveal that the high frequency switching cycle of CCD-QRLEDD has five topological states. The state's equivalent circuits are shown in Fig. 4.5.

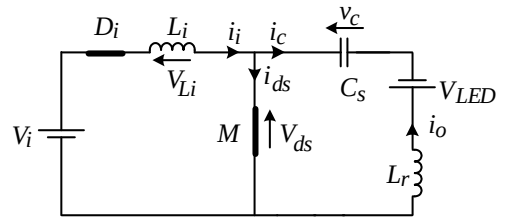
State A: t_0-t_1, see Fig. 4.5 (a), commences when M_1 is turned on. The switching occurs at zero current condition. Here, L_i begins charging from the input source, V_i, via D_i, while C_s and L_r are allowed to resonate. Here, L_r represents the magnetizing inductance of both series connected windings of the coupled inductor.

State B: t_1-t_2, see Fig. 4.5 (b), commences as D_{o1} and D_{o2} begin conducting. Hence, the coupled inductor windings are reconfigured so that both windings can discharge towards the output, V_{LED}, in parallel. The equivalent inductance of each winding is $L_r/4$. Meanwhile, C_s is clamped to the negative of the output voltage (- V_{LED}) and since M_1 is still on, the inductor L_i keeps charging.

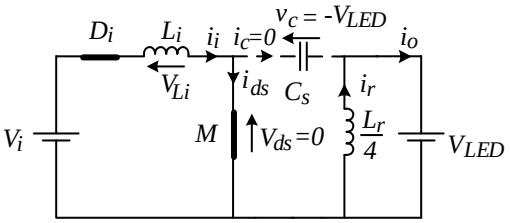
State C: t_2-t_3, see Fig. 4.5 (c), commences when the switch, M_1, is turned off, which occurs at zero voltage, v_{ds}=0, thanks to C_s snubbing. As L_i and C_s resonate the capacitor C_s is charged to a high voltage while the diodes D_{o1} and D_{o2}, conduct the resonant current to the output. In the interim, the coupled inductor keeps discharging to the output, V_{LED}. State C ends as the inductor L_i is discharged and the diode, D_i, turns off at zero current.

State D: t_3-t_4, see Fig. 4.5 (d), commences upon the turn off of the diode D_i. Both coupled inductor windings, $L_r/4$ continue to discharge the stored energy to the output while the capacitor, C_s, preserves its state. When the coupled inductor, L_r, is totally discharged, the diodes, D_{o1} and D_{o2}, turn off at zero current terminating State D.

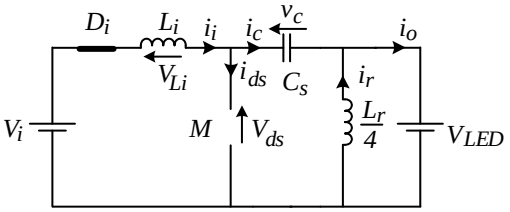
State E: t_4- t_5, see Fig. 4.5 (e), is the idle state. Here, inductors carry no current and the capacitor, C_s, preserves its state.



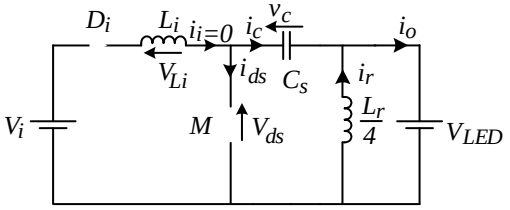
(a)



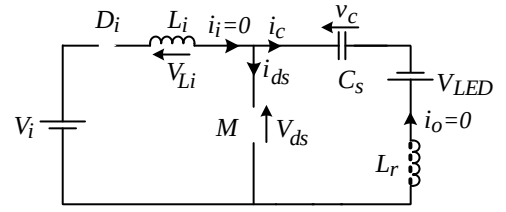
(b)



(c)



(d)



(e)

Fig. 4.5. Equivalent circuits of the topological states of the proposed CCD-QRLEDD.

(a) State A; (b) State B; (c) State C; (d) State D; (e) State E.

4.5. KEY PARAMETERS

During the on interval, $T_{on} = t_2 - t_0$, the input inductor L_i is charged by the input source, V_i, and since the charging commences from zero initial current, the inductor current rises towards

$$I_2 = i_i(t_2) = \frac{V_i}{L_i} T_{on} \qquad (4.19)$$

This can be normalized relatively to the base current $I_b = V_i/Z_{0i}$, where, $Z_{0i} = \sqrt{\frac{L_i}{C_s}}$ is defined as the characteristic impedance of the Li-Cs branch.

$$j_2 = I_2 / \left(\frac{V_i}{Z_{0i}}\right) = \left(\frac{V_i}{L_i} T_{on}\right) / \left(\frac{V_i}{Z_{0i}}\right) = \frac{T_{on}}{\sqrt{L_i C_s}} = \frac{T_{on}}{r\sqrt{L_r C_s}} = \frac{\pi}{2r} T_{on\_n} \qquad (4.20)$$

here, $r^2 = L_i/L_r$ is the inductor ratio and the normalized on time, $T_{on\_n} = 2T_{on}/\pi\sqrt{L_r C_s}$, is defined relatively to quarter of a resonant cycle of the L_r-C_s branch.

Examining the converters waveforms reveals that at $t=t_2$ the voltage across the capacitor, C_s, is $v_{Cs}(t_2) = -V_{LED}$. This can be normalized relative to the input voltage, V_i

$$m_2 = \frac{v_{Cs}(t_2)}{V_i} = -\frac{V_{LED}}{V_i} = -V_{Ln} \qquad (4.21)$$

where, $V_{Ln} = V_{LED}/V_i$ is defined as the normalized LED string voltage.

During State C, L_i-C_s branch resonates so that at the end of State C the voltage across the capacitor C_s reaches its peak value $V_m = v_{Cs}(t_3)$. Considering the equivalent circuit in Fig. 4.5 (c) and applying state plane approach, the normalized peak voltage across the capacitor, V_{mn}, can be found

$$V_{mn} = \frac{V_m}{V_i} = M_T + R \qquad (4.22)$$

Here, the normalized resonant tank voltage, M_T, is

$$M_T = \frac{V_i - V_{LED}}{V_i} = 1 - V_{Ln} \qquad (4.23)$$

and R is defined as

$$R^2 = (m_2 - M_T)^2 + j_2^2 \qquad (4.24)$$

Combining (4.25)-(4.24) yields the normalized peak capacitor voltage

$$V_{mn} = \frac{V_m}{V_i} = 1 - V_{Ln} + \sqrt{1 + \left(\frac{\pi}{2r} T_{on\_n}\right)^2} \qquad (4.25)$$

4.5.1. SWITCH VOLTAGE STRESS

During State C the diodes D_{o1} and D_{o2} conduct, see Fig. 4.5 (d), and imposes the sum of the peak capacitor voltage, V_m, and the output voltage, V_{LED}, to appear across the switch. Therefore, the normalized peak switch voltage, V_{dsmn}, can be found using (4.25)

$$V_{dsmn} = \frac{V_{dsm}}{V_i} = \frac{V_m + V_{LED}}{V_i} = 1 + \sqrt{1 + \left(\frac{\pi}{2r} T_{on\_n}\right)^2} \tag{4.26}$$

The normalized peak switch voltage (4.26) is plotted in Fig. 4.6 as a function of the normalized on time, T_{on_n}, for different inductors ratios r^2. The results are verified by simulation, and simulated points are marked on the graph. Note that the switch peak voltage is independent of the switching frequency. As it is shown in the next section, the output power can be adjusted modulating the switching frequency. Hence, the fact that frequency variations have no effect on switch voltage stress is an operational advantage of the constant T_{on} control strategy of CCD-QRLEDD.

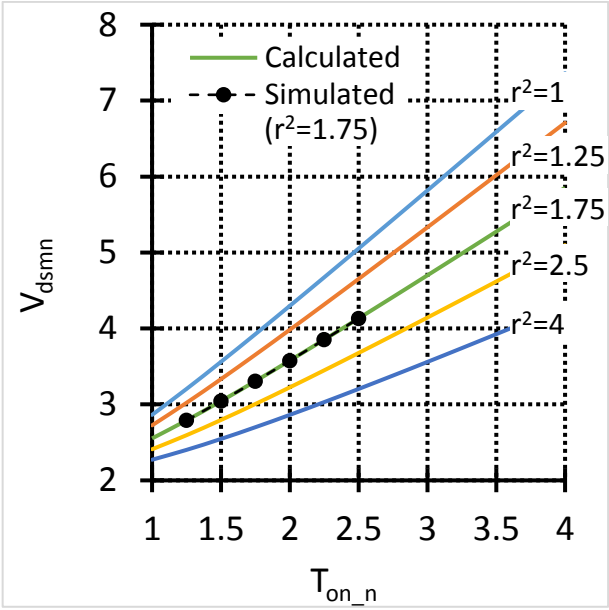


Fig. 4.6. Calculated and simulated normalized peak switch voltage, V_{dsmn}, as function of the normalized on time, T_{on_n}.

4.5.2. OUTPUT POWER

As described above, State A commences when the switch is turned on at the beginning of the switching cycle. Here, L_r-C_s branch resonates, see Fig. 4.5 (a), and the capacitor voltage changes from, $v_c(t_0) = V_m$, to $v_c(t_1) = -V_{LED}$, see Fig. 4.5 (b). The capacitor released energy, E_c, is, therefore, the difference

$$E_c = \frac{1}{2} C_s (V_m^2 - V_{LED}^2) = E_r + E_i \qquad (4.27)$$

where, E_r is the energy transferred to the resonant inductor, L_r, and E_i is the energy transferred to the LED capacitor, which replaced by V_{LED} in our analysis. Then, during States C and D, the inductor L_r discharges the acquired energy to the output.

Whereas, during State C the L_i - C_s branch resonates and the capacitor voltage is restored from $v_c(t_2) = -V_{LED}$ back to its peak voltage $v_c(t_3) = V_m$, see Fig. 4.5 (c). Since the capacitor C_s is in series with the output circuit, see Fig. 4.5 (d), the charge that flows through C_s is also delivered to the load. Note that same charge quantity

$$q_i = C_s (V_m + V_{LED}) \qquad (4.28)$$

is deposited on the load during State A and State C, see Fig. 6. Thus, the corresponding increments of energy fed to the load is

$$E_i = q_i V_{LED} = C_s (V_m + V_{LED}) V_{LED} \qquad (4.29)$$

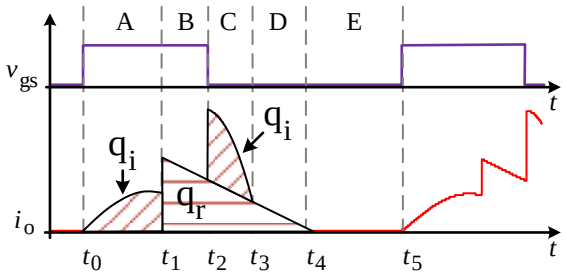


Fig. 4.7. Illustration of the charge components of the output current, i_o.

And the energy stored in the output inductor using (4.27) therefore

$$E_r = q_r V_{LED} = E_c - E_i \qquad (4.30)$$

where, q_r is the charge transferred to LED from resonant inductors.

The total energy transferred to led during switching cycle is

$$E_{LED} = (2q_i + q_r) V_{LED} = 2E_i + E_r = E_i + E_c \qquad (4.31)$$

And the average output power, P_{LED}, per switching cycle, T_s, can now be found, using $V_{dsm} = V_m + V_{LED}$ defined in (4.26)

$$P_{LED} = \frac{E_{LED}}{T_s} = \frac{E_i + E_c}{T_s} = \frac{C_s}{T_s}\left[V_{LED}V_{dsm} + \frac{V_{dsm}(V_{dsm} - 2V_{LED})}{2}\right] = \frac{1}{2} f_s C_s V_{dsm}^2 \quad (4.32)$$

here (4.31), (4.27) and (4.29) were used.

The normalized output power, P_n, can be obtained by manipulating (4.32)

$$P_n = \frac{P_{LED}}{\left(\frac{V_i^2}{Z_{0i}}\right)} = \left(\frac{f_n}{4\pi}\right) V_{dsmn}^2 \quad (4.33)$$

where, $f_s = \frac{1}{T_s}$ is the switching frequency, $f_n = \frac{f_s}{f_{0s}}$ is the normalized switching frequency and $f_{0s} = \frac{1}{2\pi\sqrt{L_i C_s}}$ is the resonant frequency of the L_i - C_s branch.

Recall that the analysis above was performed under the assumption that the input voltage to CCD-QRLEDD, V_i, is held constant, thus (4.33) is valid for dc operation conditions. When CCD-QRLEDD is operated off the utility line, additional considerations apply as described in the next sub-section.

4.5.3. AC OPERATION OF CCD-QRLEDD

Manipulating (4.33) and comparing it to power on resistor load, equivalent R_e seen from DC input can be found:

$$P_{LED} = P_n\left(\frac{V_i^2}{Z_{0i}}\right) = \frac{V_i^2}{R_e} \quad (4.34)$$

$$R_e = \frac{Z_{0i}}{P_n} \quad (4.35)$$

Given sinusoidal input voltage, we can use peak to average power ratio of $\frac{1}{2}$ to find averaged power for AC input, P_{ac}, and using V_{rms} definition for pure sinus input voltage $V_{rms} = \frac{1}{\sqrt{2}} V_i$ we get:

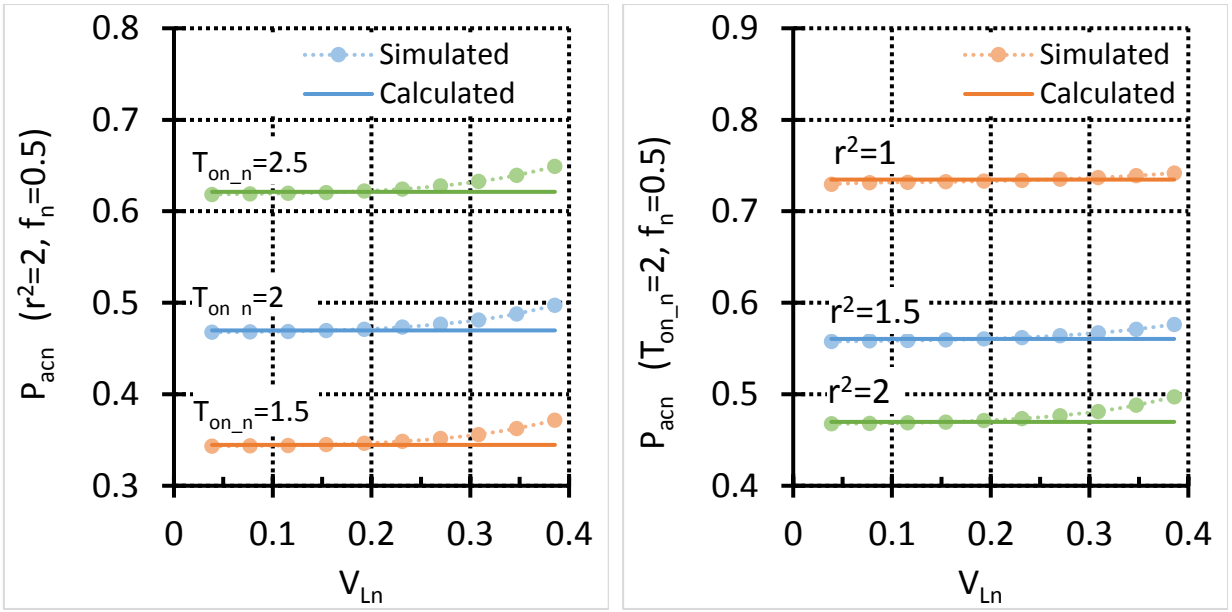
$$P_{ac} = \frac{1}{2} P_{LED\_pk} = \frac{1}{2}\left(\frac{V_i^2}{R_e}\right) = \frac{V_{rms}^2}{R_e} = P_n \frac{V_{rms}^2}{Z_{0i}} \quad (4.36)$$

Normalizing by $P_{ac0} = \frac{V_{rms}{}^2}{Z_{0i}}$ we get P_{acn}:

$$P_{acn} = \frac{P_{ac}}{P_{ac0}} = \frac{P_n {V_{rms}}^2 / Z_{0i}}{{V_{rms}}^2 / Z_{0i}} = P_n = \left(\frac{f_n}{4\pi}\right) V_{dsmn}^2 \quad (4.37)$$

So normalized averaged AC power given by the same formula as normalized DC power when normalization is done by $\frac{V_{rms}{}^2}{Z_{0i}}$. Important to note that V_{dsmn}, V_m and V_{Ln} are still normalized by the peak line voltage, V_i.

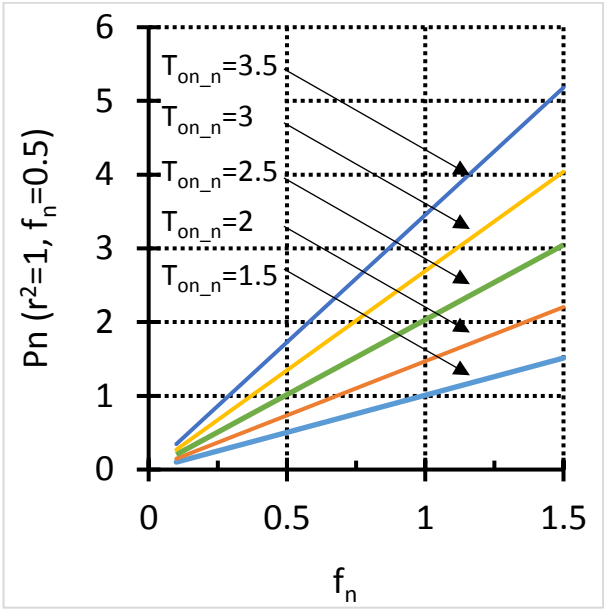
As seen from the formulas calculated powers not depend on V_{LED} but it true only when V_{Ln} below some V_{Ln_max} value that will be found below. Increasing V_{LED} or decreasing V_i (so increasing normalized LED voltage V_{Ln}) causes resonance inductor, L_r, complete discharge before finishing L_i-C_s resonance cycle and L_r begins charging in the negative direction, adding additional stages to topology period not covered in this analysis. But those stages not violate soft switching and their influence on transferred power may be neglected till it happens only for low V_i voltages during AC line period. This can be seen in following Fig. 4.8 (a) for different T_{on_n} values (r^2=2, f_n=0.5) and in Fig. 4.8 (b) for different r^2 values (T_{on_n} =2, f_n=0.5).



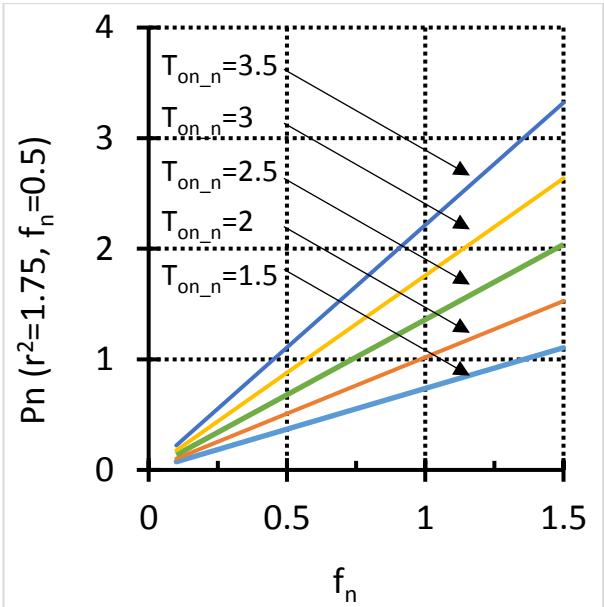
(a) (b)

Fig. 4.8 Comparison calculations to PSIM simulations of normalized AC power, P_{acn}, as function of the normalized LED voltage, V_{Ln}: (a) different normalized on time, T_{on_n} , for inductors ratio r^2=2; (b) different inductors ratios, r^2, for normalized on time, T_{on_n}=2.

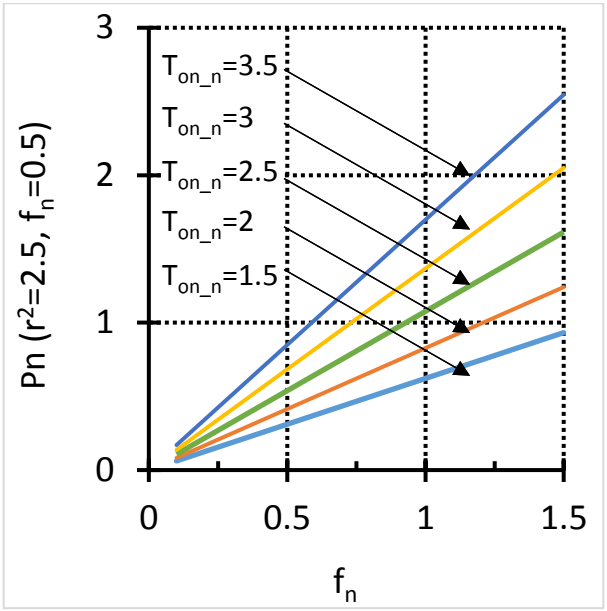
For a constant on time, T_{on_n}, the peak switch voltage, V_{dsmn}, see (4.26), is fixed. Therefore, according to (4.33) and (4.37) the output power is linear with the switching frequency, f_s, which is an additional advantage of the constant T_{on} control strategy. The normalized power, P_n, is plotted in Fig. 4.9 for selected values of inductance ratio, r^2.



(a)



(b)



(c)

Fig. 4.9. Normalized power, Pn, as function of the normalized switching frequency, fn, for different normalized on times, Ton_n. The inductors ratio, r^2, is (a) r^2=1; (b) r^2=1.75; (c) r^2=2.5.

4.5.4. Discontinuous Output Current Mode Boundary

To attain zero current, turn off condition of the output rectifier calls for maintaining discontinuous output current mode. This implies the inductor L_r be given sufficient time to complete its charge-discharge cycle. DCM condition sets an upper boundary on the switching frequency, f_{sm}. Accordingly, CCD-QRLEDD should be operated in within the specified frequency range, $f_s<f_{sm}$, where DCM prevails. DCM boundary can be found considering the waveform of i_r current, shown in Fig. 4.10.

Following considerations apply.

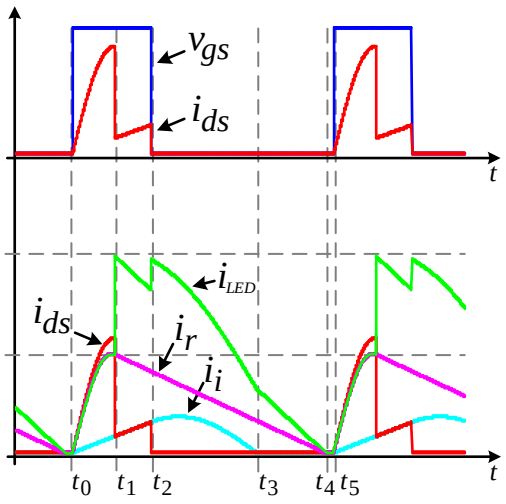


Fig. 4.10. Illustration of QRLEDD's currents in the vicinity of the DCM-CCM operation mode boundary.

The rising edge of the current i_r (here L_r charges) is due to resonant current pulse flowing in the L_r-C_s branch and is about a quarter of a resonant cycle long. To attain soft switching, the resonant pulse should be allowed to be completed before the switch is turned off. This defines the minimum switch on time, which also is the duration of State A

$$T_{on\,min} = t_A = t_1 - t_0 = \frac{\pi}{2}\sqrt{C_s L_r} \qquad (4.38)$$

During the linear discharge (States B, C, D) the coupled inductor is reconfigured so that both windings can discharge towards the output in parallel. The equivalent inductance of parallel connection is $L_r/4$. The initial value, I_{om}, of which the coupled inductor starts its discharge can be found from energy conservation considerations using (4.30) as

$$I_{om} = \sqrt{\frac{2}{(L_r/4)}E_r} = 2\sqrt{\frac{C_s}{L_r}[(V_m^2 - V_{LED}^2) - 2V_{LED}(V_m + V_{LED})]} =$$

$$2\sqrt{\frac{C_s}{L_r}[(V_m - V_{LED})^2 - 4V_{LED}^2]} = 2\sqrt{\frac{C_s}{L_r}[V_{dsm}^2 - 4V_{dsm}\,V_{LED}]} \qquad (4.39)$$

Thus, the duration of the linear discharge interval, t_{BCD}, which is the combined duration of States B, C, and D, is given by

$$t_{BCD} = t_4 - t_1 = \frac{L_r/4}{V_{LED}} I_{om} = \frac{\sqrt{C_s L_r\left(V_{dsm}^2 - 4V_{dsm}\,V_{LED}\right)}}{2\,V_{LED}} \qquad (4.40)$$

Combining (4.38) and (4.40) the maximum allowable switching frequency, f_{sm}, for DCM operation can be derived

$$f_{sm} = \frac{1}{t_A + t_{BCD}} = \frac{2}{\sqrt{C_s L_r}}\left[\pi + \sqrt{\left(\frac{V_{dsm}}{V_{LED}}\right)^2 - 4\frac{V_{dsm}}{V_{LED}}}\right]^{-1} \qquad (4.41)$$

Normalizing the last equation yields

$$f_{smn} = \frac{f_{sm}}{f_{0s}} = 4\pi r\left[\pi + \sqrt{\left(\frac{V_{dsmn}}{V_{Ln}}\right)^2 - 4\frac{V_{dsmn}}{V_{Ln}}}\right]^{-1} \qquad (4.42)$$

here, V_{dsmn}, V_{Ln}, r, and f_{os} are as defined above. The result and comparison with PSIM simulation are plotted in Fig. 4.11.

4.6. SIMULATION AND EXPERIMENTAL VERIFICATION

Table 4.1. CCD QRLEDD Experimental Parameters

Parameter	*Value*
V_i	110 Vac 60Hz
V_{LED}	20W COB module 31.5 V @ 0.638 A
$2C_s$	2.67 nF (2.2 nF B81123C1222M189 || 0.47 nF VY1471K31Y5UQ63V0)
M	ST STP11N65M2 (R_{ds}=670mOhm, E_{oss}=1.6μJ @ 400V)
L_i	108 μHr EPCOS B65813J0000R049 (RM10 N49 ferrite, 31 turns)
$\frac{L_r}{4}$	2x 27 μHr EPCOS B65813J0000R049 (RM10 N49 ferrite, 2x 24 turns in parallel)
D_i	Cree C3D02060F SiC Diode
D_{o1}, D_{o2}	ST STTH5L06RL
C_o	220 μF Electrolytic WIMA EEU-FR1J221L
f_{sm}	300 kHz
T_{on}	770 ns

Experimental CCD QRLEDD was build and tested. The parameters of the experimental prototype were according to Table 4.1.

Measured and simulated parameters and waveforms of the CCD QRLEDD are illustrated in Fig. 4.11 and Fig. 4.12. Good agreement is found.

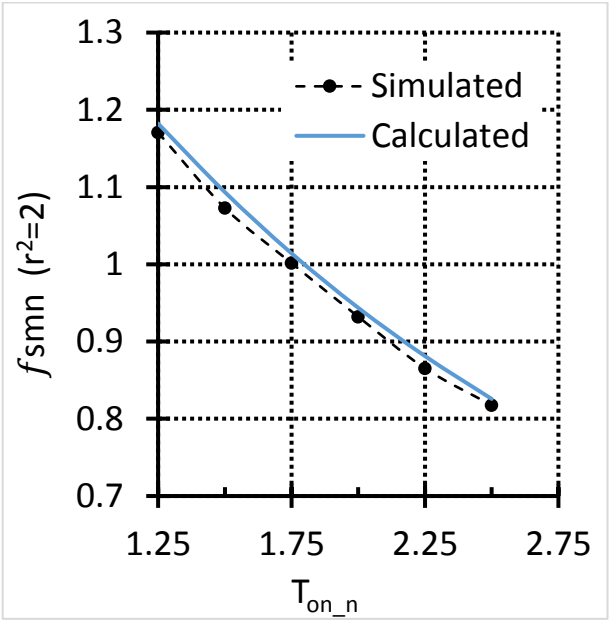


Fig. 4.11. Comparison of theoretically predicted and simulated maximal normalized switching frequency, fnm, as function of the normalized on time, Ton_n, for $r^2=2$.

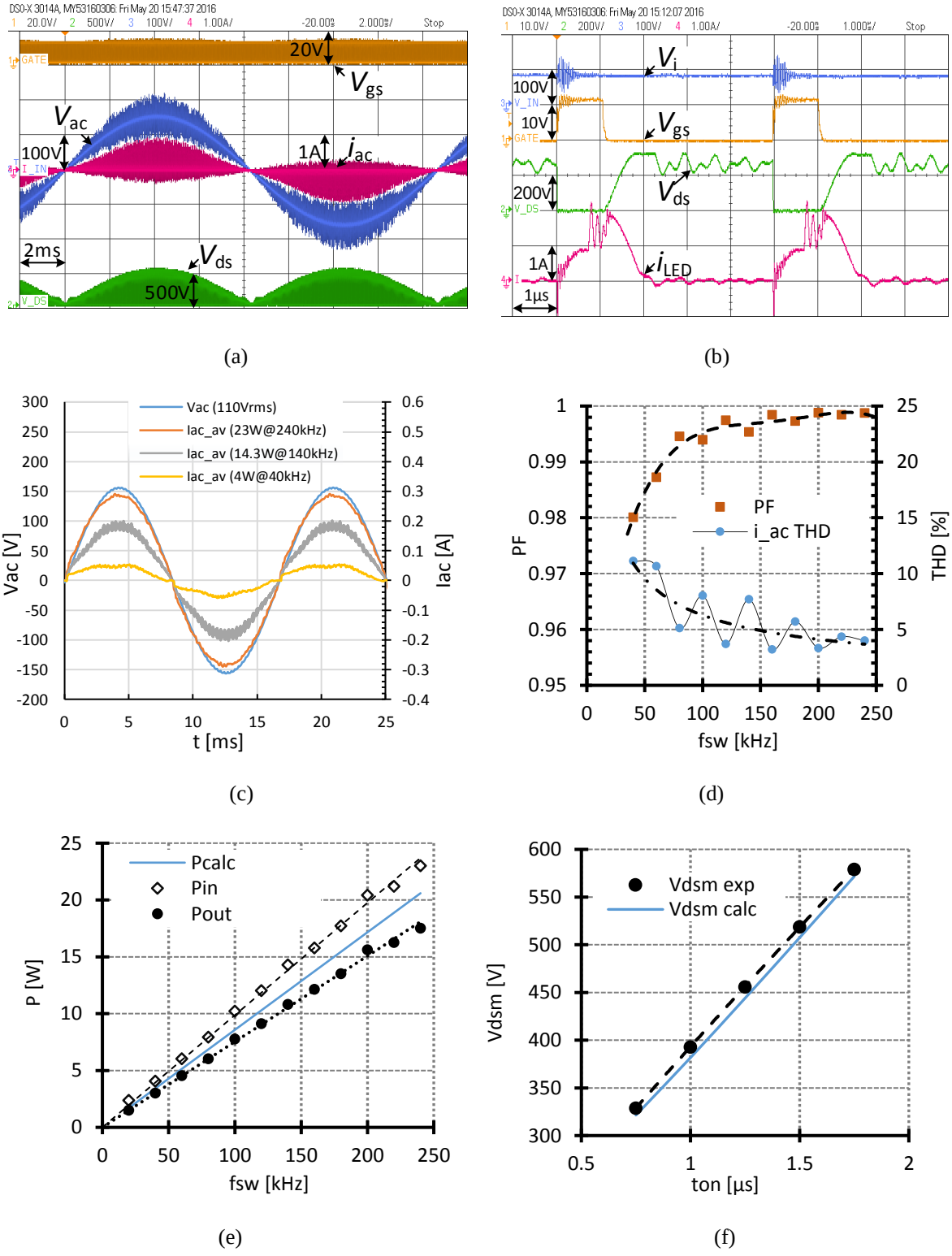


Fig. 4.12. Experimental results: (a) input port waveforms on the line period scale;
(b) key waveforms on the switching period scale;
(c) line voltage and averaged line current at different switching frequencies (power levels);
(d) THD and PF performance indexes;
(e) comparison of the theoretically predicted, Pcalc, and measured power, Pin, Pout, as function of switching frequency;
(f) comparison of predicted vs. measured peak switch voltage.

4.7. EFFICIENCY IMPROVEMENT

To check the possibility of efficiency improvement, a lower frequency topology was tested. 2Cs capacitors were replaced by a single Cs capacitor (removing isolation) . Updated parameters are presented in Table 4.2. And a comparison of the experimental results before and after change may be found in Fig. 4.13.

Table 4.2. CCD QRLEDD Efficiency Experiment changes

Parameter	*Value*
C_s	3.2 nF (2.2 nF B81123C1222M189 || 1 nF R73UI11004000J)
L_i	387 μHr EPCOS B65813J0000R049 (RM10 N49 ferrite, 100 turns)
$\frac{L_r}{4}$	2x 47 μHr EPCOS B65813J0000R049 (RM10 N49 ferrite, 2x 47 turns in parallel)
T_{on}	2.25 μs

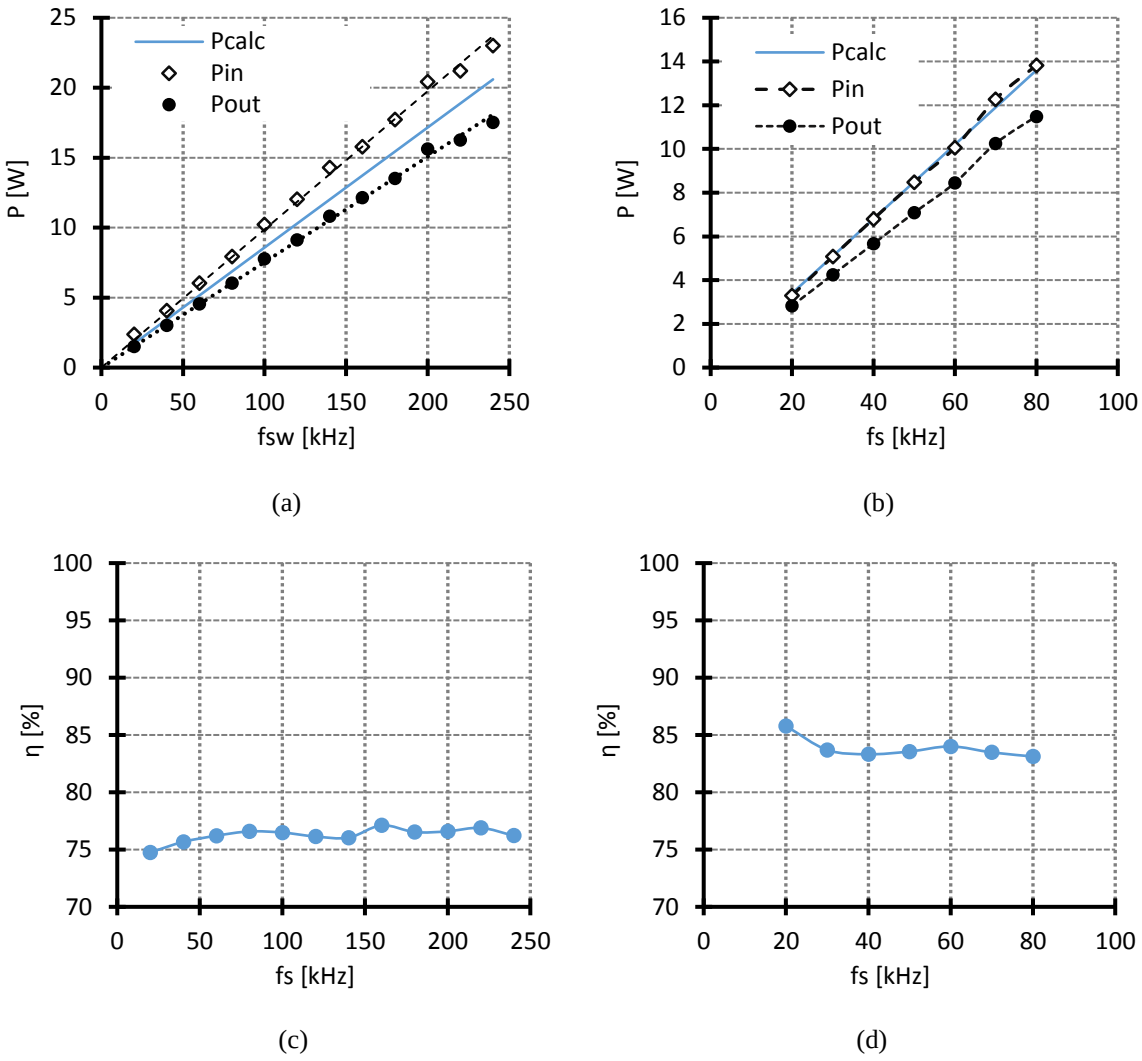


Fig. 4.13. Experimental results:
(a) Powers before the change;
(b) Powers after the change;
(c) Efficiency before the change;
(d) Efficiency after the change.

CHAPTER 5

SUMMARY

5.1. SUMMARY & CONCLUSIONS

This thesis reports on a theory, simulation and experimental results of the selected topologies from a family Quasi-Resonant LED Drivers. The significant merits of the analyzed topologies include single ground referenced switch and a gate driver, inherent passive power balance of multiple LED strings, capacitive isolation feature, the large voltage step down, low line current distortion, soft switching, and high frequency operation. Major performance indexes were derived theoretically and evaluated by both simulation and experiment. Good agreement was found.

The brightness of a LED strings can be controlled by modulating either the switch on time or frequency. Burst mode dimming can also be considered.

This family combines PFC, power conversion and current balancing into the single isolated stage. As described in the introduction, usually a smaller bank capacitor, C_B, between PFC and power converter helps smooth double line-frequency ripple by utilizing regulation capabilities of the power converter. Combining PFC with power conversion helps reduce components count and associated with its size, price, and improved simplicity and efficiency. On the other hand, it removes bank capacitor, C_B, requiring larger output capacitors or usage of a bi-directional DC-DC converter to replace it [42], canceling out part of the advantages.

In current work, we switched to not certified as class Y capacitors. The reason is that available class Y capacitors usually have big dissipation factor to dump EMI oscillations and hence causing big losses in power transfer usage. We kept capacitors value as small as possible, in the same range as used in EMI bridging but did not measure a touch current (TC) itself as it depends on EMI filter in use and the TC was not in the scope of this work.

In conclusion, this family of LED Drivers gives a simple and low-cost alternative to conventional LED Drivers making it possible to implement Safety Extra Low Voltage (SELV) protection from electric shock without the usage of a magnetic isolation transformer.

5.2. PROPOSED FUTURE WORK

Based on obtained results following direction for further investigation proposed:

5.2.1. EFFICIENCY IMPROVEMENTS

A simulation of losses in Fig. 3.16 suggests that output diodes play a critical role in overall efficiency. Their influence may be diminished using increased isolation capacitors. Higher series capacitors reduce an influence of parasitic capacitances of diodes and switch. However, increasing the isolation capacitance also increases a TC that may be mitigated by a CM choke.

Influence of a voltage drop on output diodes may be addressed by increased output voltage. In this case, a crossing of Safety Extra Low Voltage (SELV) border will require the use of protection against electric shock by other means, e.g., safety insulation or grounded enclosure. Applying additional safety protections reduces the inherent advantage of isolation but given the low component count and other advantages suggests competition with other non-isolated topologies.

Another approach to the voltage drop is applying synchronous rectifier (SR) as was already proposed Shmilovitz *et al.*, 2016 [38], see Fig. 1.10 (f). This method may be applied also for CD and CCD versions of topologies in Fig. 1.10 (c) and (d) using 2 SR switches. Moreover, in case of CCD, see Fig. 1.10 (d), by slightly increasing the bottom coupled inductor (relative to the upper to make a voltage difference above diode drop) will cause discharging of accumulated energy only via the bottom circuit. In this case, only single ground referenced SR switch in parallel with the bottom diode, D_6, is required.

5.2.2. EMI FILTER DESIGN AND TOUCH CURRENT MEASUREMENTS

Wide switching frequency variation possesses difficulty on EMI filter design to meet EMC requirements at all working frequencies across the range. This was not tested and investigated in current work. Additionally, measurements of TC and required CM choke to keep it in allowed range proposed for future work.

5.2.3. PRIMARY SIDE ONLY CLOSED LOOP VERSION

In current work, all topologies operated in open loop with manual control by a signal generator. Closed loop control may be applied. Recalling that an output power depends only on a switching frequency, peak switch voltage and isolation capacitors values, see (3.22). Given, that isolation capacitors preserve their value then a line and load variations may be detected monitoring the peak switch voltage, V_{dsm}, and compensated adjusting the switch on time, T_{on}, and the switching frequency, f_s. All these parameters available on a primary side of the converter, reducing the need for optocoupler or other means to close the loop across the isolation barrier.

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APPENDICES

A.1. MATLAB 3D PLOTS GENERATION

```
close all;


%% DCDC new analysis
POINTS_PER_INT = 100;


r=sqrt(3);
Li = 79e-6; %[Hr]
Cs = 8e-9;  %[F]
w0i = 1./sqrt(Li*Cs);
w0r = r*w0i;
Tbase = 2*pi/w0i;

Vln = 0.4; % Vled/Vin
tn = 1.3/4; % Ton/Tbase
Ton = tn*Tbase; %[s]


Vmn = 1-Vln+sqrt(1+(2*pi*tn)^2);


tA = 1./w0r*(pi/2+asin(Vln/Vmn));

tB = Ton - tA;

tC = 1/w0i*(pi-atan(2*pi*tn));

tD = sqrt(Vmn^2 - Vln^2)/Vln/w0r - tB - tC;

t0=0;
t1=tA;
t2=tA+tB;
t3=tA+tB+tC;
t4=tA+tB+tC+tD;

Mt = 1-Vln;
Ri = sqrt(1+(w0i*Ton)^2);

%% intervals definition
% structure of the arrays: [ji; jr; mc;]

t = linspace(0,t1,POINTS_PER_INT);
a = [ w0i * t;
     Vmn * sin( w0r * t);
     Vmn * cos( - w0r * t)];

t = linspace(t1,t2,POINTS_PER_INT);
b = [ w0i * (t);
    sqrt(Vmn^2 - Vln^2) - Vln*w0r*(t-t1);
    -Vln*ones(1,POINTS_PER_INT)];

t = linspace(t2,t3,POINTS_PER_INT);
c = [Ri * sin(w0i*tC-w0i*(t-t2));
    sqrt(Vmn^2 - Vln^2) - Vln*w0r*(t-t1);
    Mt + Ri * cos(w0i*tC-w0i*(t-t2)) ];

t = linspace(t3,t4,POINTS_PER_INT);
d = [zeros(1,POINTS_PER_INT);
    sqrt(Vmn^2 - Vln^2) - Vln*w0r*(t-t1);
    Vmn*ones(1,POINTS_PER_INT)];



%% main curve

line_width = 2;
```

```
%% prepare axes for plotting:
%
fig = figure();
ax = gca();
view(ax, [138, 25]);
axis equal
hold on

ax_max = 4;
ax_min = -2;

mrkrs = {'none','+','o','^','v'};
msizes = ones(1,5)*7;
msizes(2)=msizes(2)*1.7;

clrs = [228,26,28;
55,126,184;
77,175,74;
255,127,0;
152,78,163;]./255;

clrs = clrs*0.9;


%% Plot 3d lines:
main_line = plot3(ax,a(1,:),a(2,:),a(3,:),'LineWidth',line_width,'Color',clrs(1,:));
main_line = plot3(ax,b(1,:),b(2,:),b(3,:),'LineWidth',line_width,'Color',clrs(2,:));
main_line = plot3(ax,c(1,:),c(2,:),c(3,:),'LineWidth',line_width,'Color',clrs(3,:));
main_line = plot3(ax,d(1,:),d(2,:),d(3,:),'LineWidth',line_width,'Color',clrs(4,:));
main_line = plot3(ax,d(1,end),d(2,end),d(3,end),'LineWidth',line_width,'Color',clrs(5,:));


ls = '1.5';
grid on;

% add axes arrows:
funcs.arrow3([ax_min,0,0],[ax_max,0,0],ls,2)
funcs.arrow3([0,ax_min,0],[0,ax_max,0],ls,2)
funcs.arrow3([0,0,ax_min],[0,0,ax_max],ls,2)


ax = gca;
ax.GridAlpha = 0.3;
x=0.3;
ax.GridColor = [x, x, x];



%% axis projections
proj_offset = ax_min;% -3; % inf;
prj_ax_min = -1; %ax_min + 0.5;
prj_ax_max = ax_max - 0.5;

ls = '1-0.6'; %line style
% add axes of projections:
funcs.arrow3([proj_offset,0,prj_ax_min],[proj_offset,0,prj_ax_max],ls,2)
funcs.arrow3([proj_offset,prj_ax_min,0],[proj_offset,prj_ax_max,0],ls,2)

funcs.arrow3([prj_ax_min,proj_offset,0],[prj_ax_max,proj_offset,0],ls,2)
funcs.arrow3([0,proj_offset,prj_ax_min],[0,proj_offset,prj_ax_max],ls,2)

funcs.arrow3([0,prj_ax_min,proj_offset],[0,prj_ax_max,proj_offset],ls,2)
funcs.arrow3([prj_ax_min,0,proj_offset],[prj_ax_max,0,proj_offset],ls,2)


%% plot projections

zr=zeros(size(a(1,:)))+proj_offset;

main_line = plot3(ax,a(1,:),a(2,:),zr,'LineWidth',line_width,'Color',clrs(1,:));
main_line = plot3(ax,b(1,:),b(2,:),zr,'LineWidth',line_width,'Color',clrs(2,:));
main_line = plot3(ax,c(1,:),c(2,:),zr,'LineWidth',line_width,'Color',clrs(3,:));
main_line = plot3(ax,d(1,:),d(2,:),zr,'LineWidth',line_width,'Color',clrs(4,:));

main_line = plot3(ax,a(1,:),zr,a(3,:),'LineWidth',line_width,'Color',clrs(1,:));
main_line = plot3(ax,b(1,:),zr,b(3,:),'LineWidth',line_width,'Color',clrs(2,:));
main_line = plot3(ax,c(1,:),zr,c(3,:),'LineWidth',line_width,'Color',clrs(3,:));
```

```
main_line = plot3(ax,d(1,:),zr,d(3,:),'LineWidth',line_width,'Color',clrs(4,:));

main_line = plot3(ax,zr,a(2,:),a(3,:),'LineWidth',line_width,'Color',clrs(1,:));
main_line = plot3(ax,zr,b(2,:),b(3,:),'LineWidth',line_width,'Color',clrs(2,:));
main_line = plot3(ax,zr,c(2,:),c(3,:),'LineWidth',line_width,'Color',clrs(3,:));
main_line = plot3(ax,zr,d(2,:),d(3,:),'LineWidth',line_width,'Color',clrs(4,:));


%% add texts labels and legend
font = 14;
xlabel('j_i','FontSize',font)
ylabel('j_r','FontSize',font)
zlabel('m_C','FontSize',font)

dt = 0.2;
text(ax_max+dt, 0, 0, ['j_i',' '],'FontSize',font);
text(0, ax_max+dt, 0, ['j_r',' '],'FontSize',font);
text(0, 0, ax_max+dt, ['m_C',' '],'FontSize',font);


leg ={  'State A',...
        'State B',...
        'State C',...
        'State D',...
        'State E' };
legend(leg);

%view_n = inf;
xlim([proj_offset,inf])
ylim([proj_offset,inf])
zlim([proj_offset,inf])


%% create 2d plots of projections:
%hold off

% [ji; jr;] - less interesting
figure;
%jrji_line=plot(ji,jr,'c');
hold on;
jrji_line = plot(a(1,:),a(2,:),'LineWidth',line_width,'Color',clrs(1,:));
jrji_line = plot(b(1,:),b(2,:),'LineWidth',line_width,'Color',clrs(2,:));
jrji_line = plot(c(1,:),c(2,:),'LineWidth',line_width,'Color',clrs(3,:));
jrji_line = plot(d(1,:),d(2,:),'LineWidth',line_width,'Color',clrs(4,:));
grid on;
axis equal;
ls = 'k-1';
as = 1;
funcs.arrow3([0,prj_ax_min],[0,prj_ax_max],ls,as)
funcs.arrow3([prj_ax_min,0],[prj_ax_max,0],ls,as)
xlim([prj_ax_min,inf])
ylim([prj_ax_min,inf])
legend(leg);


%[ji; mc;]
figure;
hold on;
%jimc_line=plot(ji,mc,'g');
h(1) =
plot(a(1,:),a(3,:),'LineWidth',line_width,'Color',clrs(1,:),'Marker',mrkrs{1},'MarkerFaceColor
',clrs(1,:));

% plot line
jimc_line = plot(b(1,:),b(3,:),'LineWidth',line_width,'Color',clrs(2,:));

% plot markers
dil=50;
plot(b(1,dil:dil:end-dil),b(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(2,:),'Marker',mrkrs{2},'MarkerFace
Color',clrs(2,:), 'MarkerSize',msizes(2));

% create legend entry
h(2)=plot(inf,inf,'LineWidth',line_width,'Color',clrs(2,:),'Marker',mrkrs{2},'MarkerFaceColor'
,clrs(2,:), 'MarkerSize',msizes(2));

% plots line/markers/creates legend entry
jimc_line = plot(c(1,:),c(3,:),'LineWidth',line_width,'Color',clrs(3,:));
dil=20;
```

```
plot(c(1,dil:dil:end-dil),c(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(3,:),'Marker',mrkrs{3},'MarkerFace
Color',clrs(3,:), 'MarkerSize',msizes(3));
h(3)=plot(inf,inf,'LineWidth',line_width,'Color',clrs(3,:),'Marker',mrkrs{3},'MarkerFaceColor'
,clrs(3,:), 'MarkerSize',msizes(3));

% plots line/markers/creates legend entry
jimc_line = plot(d(1,:),d(3,:),'LineWidth',line_width,'Color',clrs(4,:),'Marker',mrkrs{4});
dil=50;
plot(d(1,dil:dil:end-dil),d(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(4,:),'Marker',mrkrs{4},'MarkerFace
Color',clrs(4,:), 'MarkerSize',msizes(4));
h(4)=plot(inf,inf,'LineWidth',line_width,'Color',clrs(4,:),'Marker',mrkrs{4},'MarkerFaceColor'
,clrs(4,:), 'MarkerSize',msizes(4));

% plots line with markers and uses it as legend entry
h(5)=plot(d(1,end),d(3,end),'LineWidth',line_width,'Color',clrs(5,:),'Marker',mrkrs{5},'Marker
FaceColor',clrs(5,:), 'MarkerSize',msizes(5));

% adds axes, grid and adjusts view
grid on; axis equal; hold on;
funcs.arrow3([prj_ax_min, 0],[prj_ax_max, 0],ls,as)
funcs.arrow3([0, prj_ax_min],[0, prj_ax_max],ls,as)
xlim([prj_ax_min,inf])
ylim([prj_ax_min,inf])

legend(h,leg,'Location','NW');

ax = gca;
ax.XDir='reverse';
ax.GridAlpha = 0.3;
x=0.3;
ax.GridColor = [x, x, x];

dt = 0.25;
text( prj_ax_max-dt/1.5, -dt, ['j_i',' '],'FontSize',font);
text( -dt/2, prj_ax_max-dt, ['m_C',' '],'FontSize',font);

% [jr; mc;]
figure;
hold on;

% plots line with markers and uses it as legend entry
h(1) =
plot(a(2,:),a(3,:),'LineWidth',line_width,'Color',clrs(1,:),'Marker',mrkrs{1},'MarkerFaceColor
',clrs(1,:));

% plots line/markers/creates legend entry
dil=1;
jrmc_line = plot(b(2,1:dil:end),b(3,1:dil:end),'LineWidth',line_width,'Color',clrs(2,:));
dil=50;
jrmc_line = plot(b(2,dil:dil:end-dil),b(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(2,:),'Marker',mrkrs{2},'MarkerFace
Color',clrs(2,:), 'MarkerSize',msizes(2));
h(2)=plot([inf],[inf],'LineWidth',line_width,'Color',clrs(2,:),'Marker',mrkrs{2},'MarkerFaceCo
lor',clrs(2,:), 'MarkerSize',msizes(2));

% plots line/markers/creates legend entry
dil=1;
jrmc_line = plot(c(2,1:dil:end),c(3,1:dil:end),'LineWidth',line_width,'Color',clrs(3,:));
dil=20;
jrmc_line = plot(c(2,dil:dil:end-dil),c(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(3,:),'Marker',mrkrs{3},'MarkerFace
Color',clrs(3,:), 'MarkerSize',msizes(3));
h(3)=plot(inf,inf,'LineWidth',line_width,'Color',clrs(3,:),'Marker',mrkrs{3},'MarkerFaceColor'
,clrs(3,:), 'MarkerSize',msizes(3));

% plots line/markers/creates legend entry
dil=1;
jrmc_line = plot(d(2,1:dil:end),d(3,1:dil:end),'LineWidth',line_width,'Color',clrs(4,:));
dil=50;
jrmc_line = plot(d(2,dil:dil:end-dil),d(3,dil:dil:end-
dil),'LineStyle','none','LineWidth',line_width,'Color',clrs(4,:),'Marker',mrkrs{4},'MarkerFace
Color',clrs(4,:), 'MarkerSize',msizes(4));
h(4) =
plot(inf,inf,'LineWidth',line_width,'Color',clrs(4,:),'Marker',mrkrs{4},'MarkerFaceColor',clrs
(4,:), 'MarkerSize',msizes(4));

% plots line with markers and uses it as legend entry
```

```
h(5) =
plot(d(2,end),d(3,end),'LineWidth',line_width,'Color',clrs(5,:),'Marker',mrkrs{5},'MarkerFaceC
olor',clrs(5,:), 'MarkerSize',msizes(5));

% adds axes, grid and adjusts view
grid on; axis equal; hold on;
funcs.arrow3([0,prj_ax_min ],[0,prj_ax_max ],ls,as)
funcs.arrow3([prj_ax_min,0 ],[prj_ax_max,0 ],ls,as)
xlim([prj_ax_min,inf])
ylim([prj_ax_min,inf])
legend(h,leg);
dt = 0.25;
text( prj_ax_max-dt/1.5, -dt, ['j_r',' '],'FontSize',font);
text( dt/2, prj_ax_max-dt, ['m_C',' '],'FontSize',font);

ax = gca;
ax.GridAlpha = 0.3;
x=0.3;
ax.GridColor = [x, x, x];
```

A.2. PROTOTYPE BOARD SCHEMATICS AND PCB

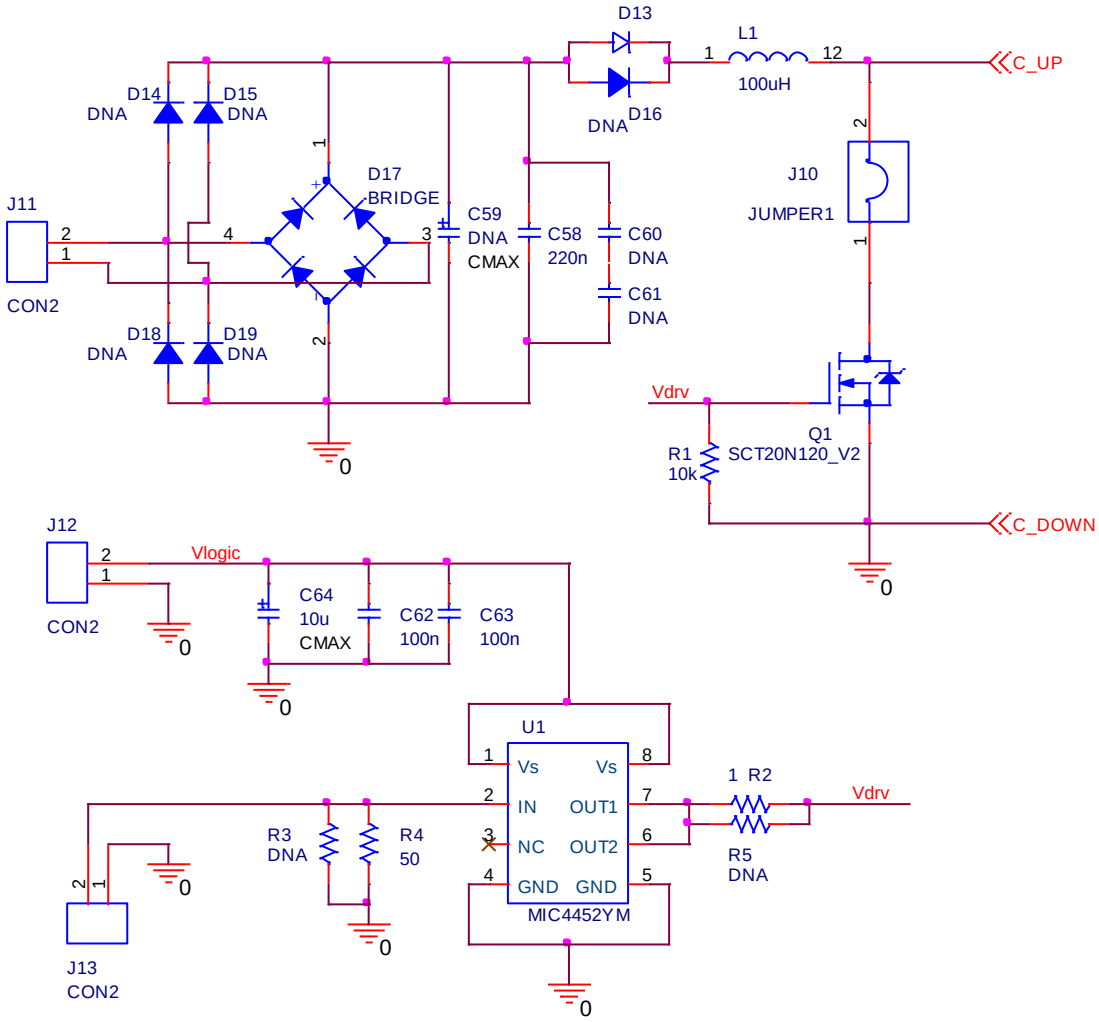

Fig. 5.1. Input stage and FET driver

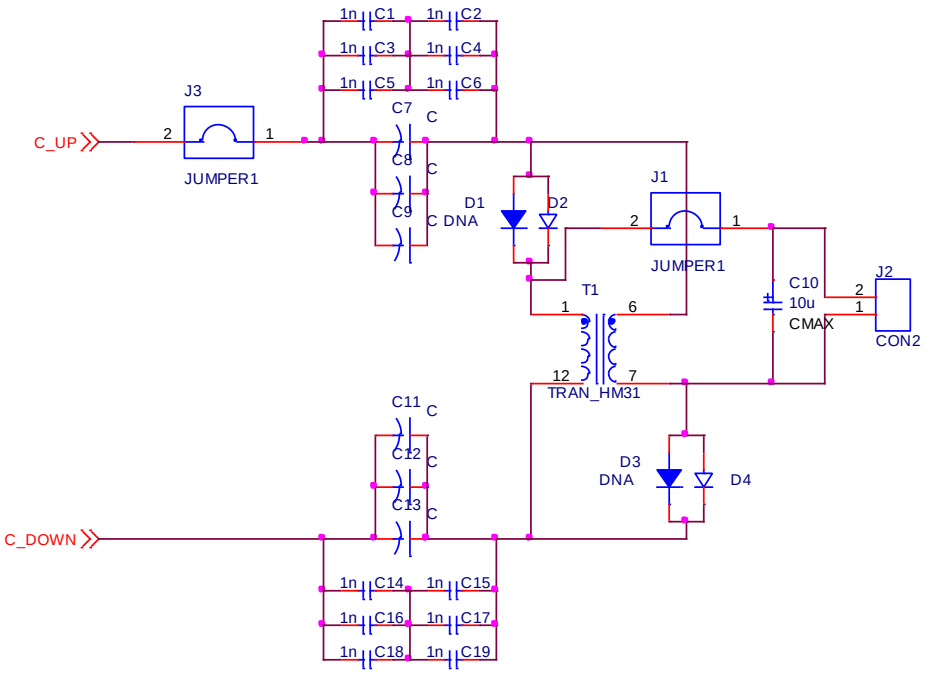

Fig. 5.2. String 1

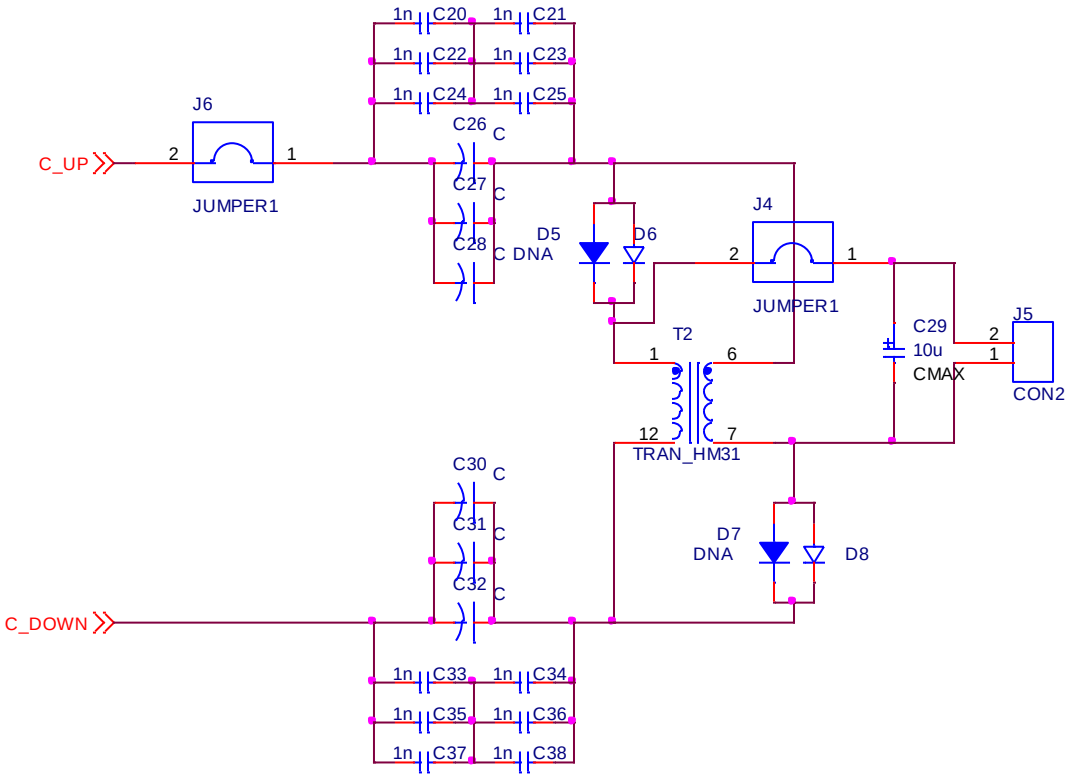

Fig. 5.3. String 2

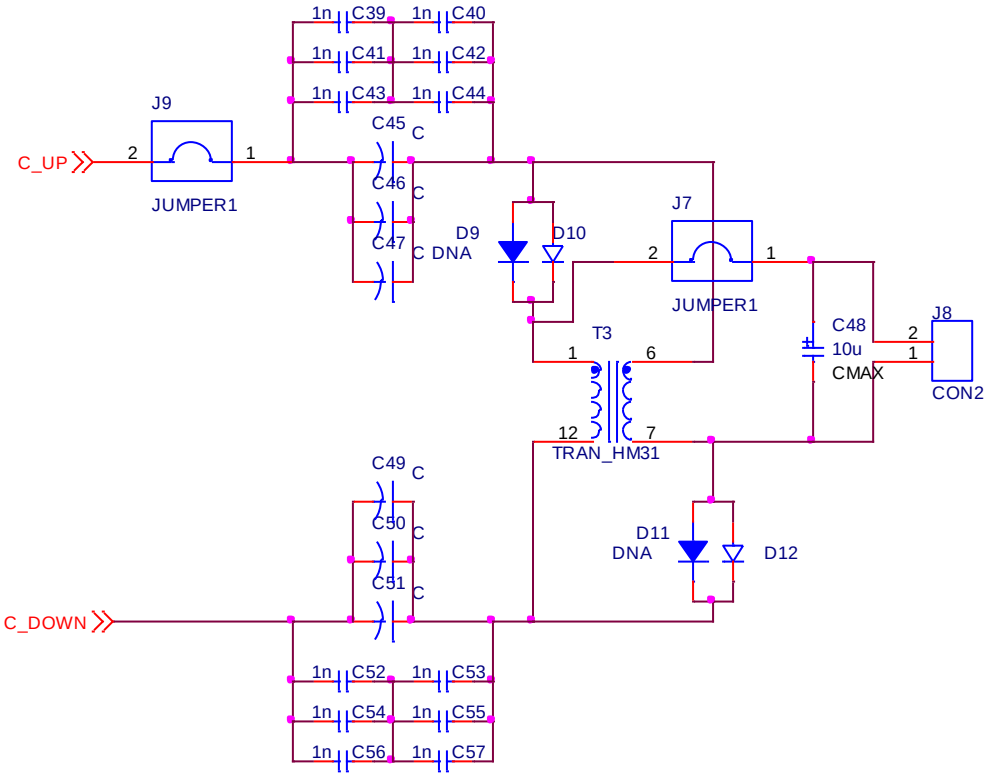

Fig. 5.4. String 3

Printed Circuit Board (PCB):

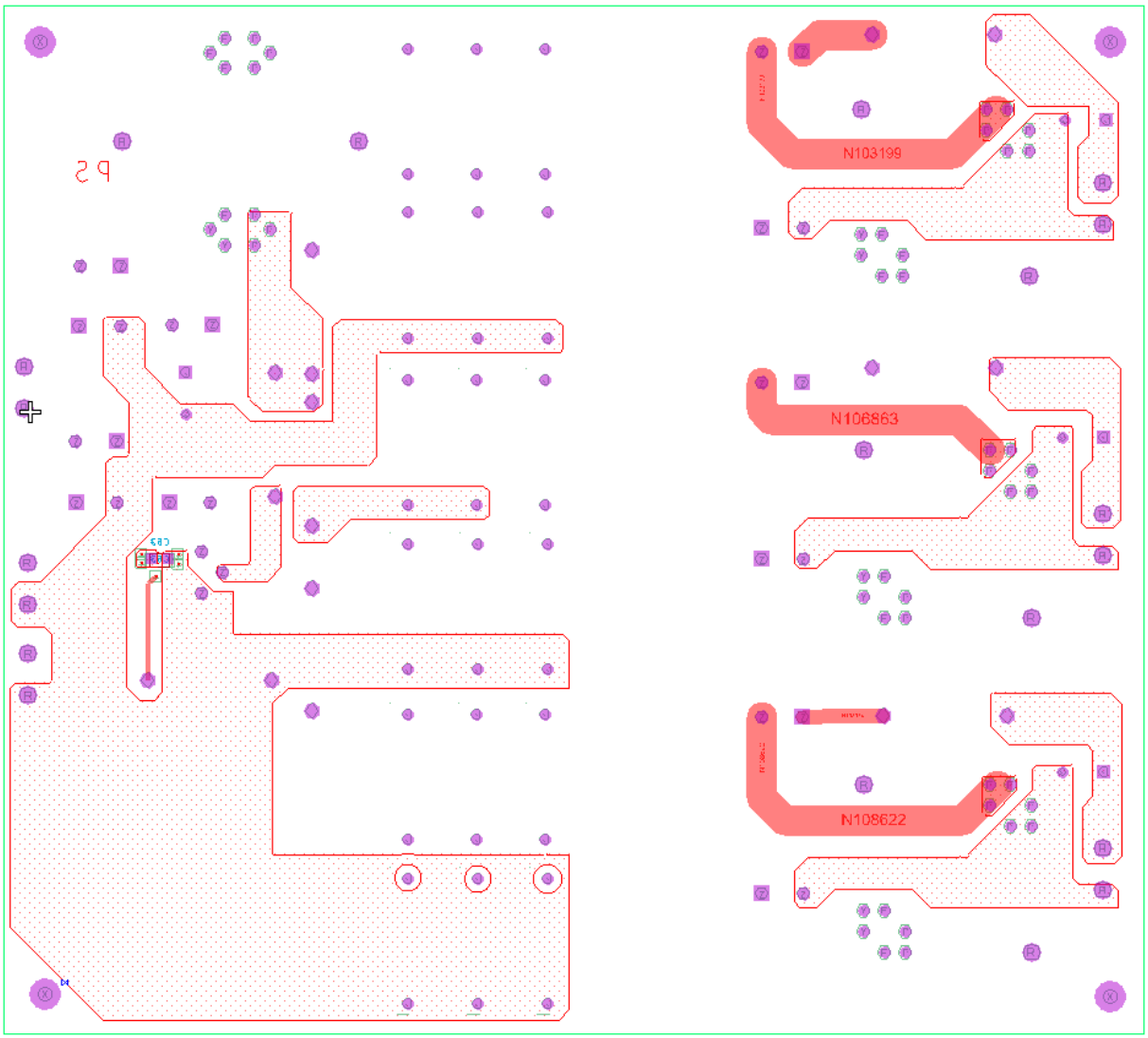

Fig. 5.5. PCB PS side

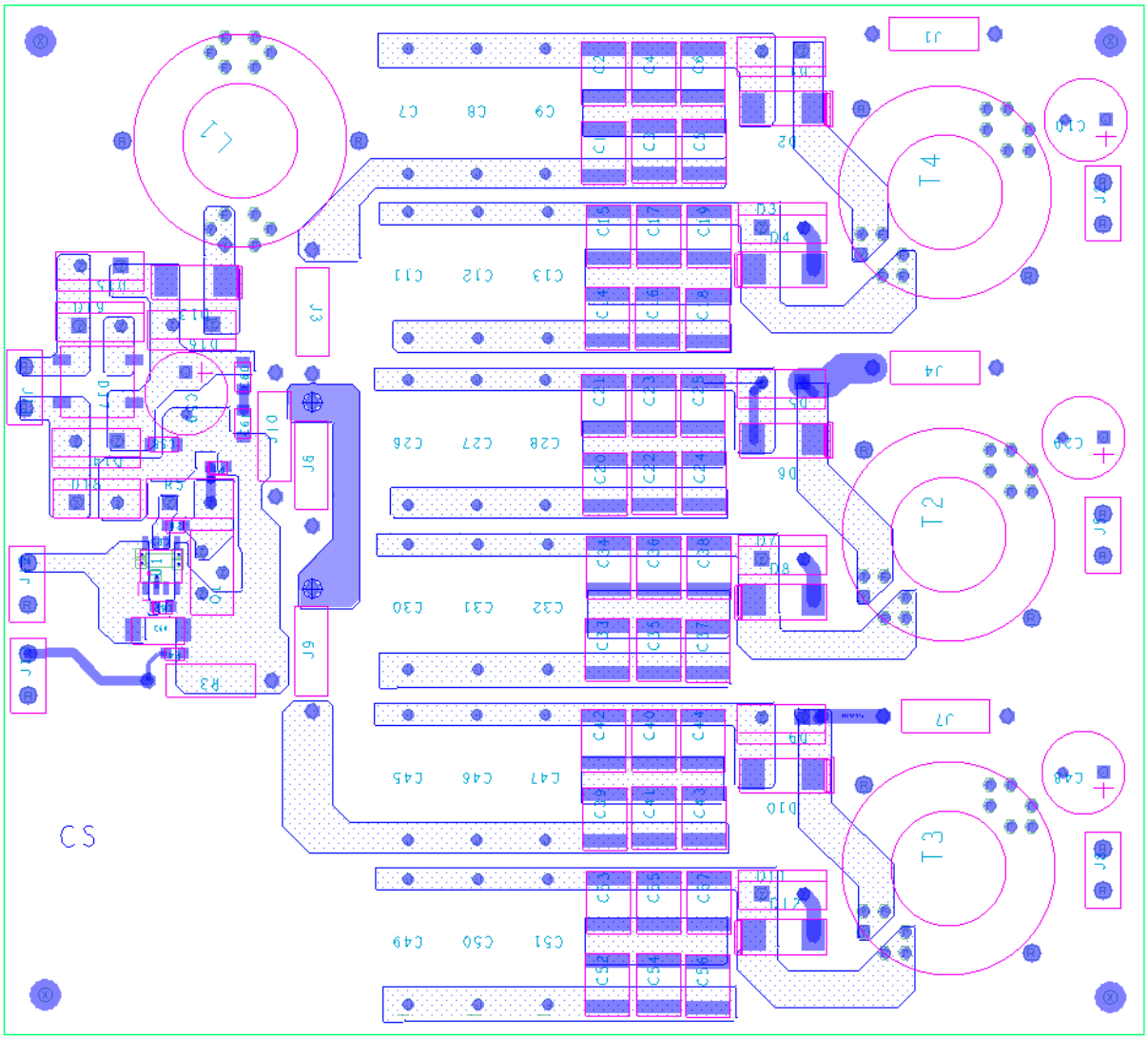

Fig. 5.6. PCB CS side

תקציר

בעשור אחרון יש עליה בפופולריות של תאורה המבוססת על דיודות פולטות אור (LED) כתוצאה מיתרונותיה הרבים כגון חסכון באנרגיה, משך חיים ארוך וידידותיות לסביבה. עם עליה זו עולה גם הצורך בממירים ממתח משתנה (AC) של הרשת חשמל למתח ישר (DC) מבוקר זרם המתאים להפעלת LED-ים. ממירים אלה נקראים דוחפי LED.

בין התכונות הרצויות של דוחפי LED: נצילות גבוה, משך חיים ארוך, גורם הספק גבוה ועיוותים הרמוניים נמוכים בזרם הנצרך, יכולת להזין מספר רב של ה-LED-ים וכל זה במחיר נמוך ובצורה בטוחה. אחת הדרכים להשיג את זה היא להקטין את כמות הדרגות במבנה של דוחף LED-ים על-ידי איחודם.

עבודה זו מנתחת ובודקת בסימולציה ובצורה מעשית את משפחת דוחפי LED שמאחדת את דרגת תיקון גורם הספק (PFC), דרגת המרה ודרגת חלוקה של זרם יציאה לדרגה אחת. דרגה זאת משיגה בנוסף בידוד קיבולית בין כניסה ליציאה המאפשר לפשט הגנה מפני התחשמלות.

משפחת דוחפי LED שבמרכז עבודה בעלת יתרונות נוספים כמו מספר רכיבים קטן, שימוש במתג בודד מיוחס לאדמה שמוריד צורך בדוחף שער מבודד. קבלי צימוד משתתפים במעגלי תהודה גם עם הסליל כניסה וגם עם סליל יציאה וגורמים למיתוג רך של כל המוליכים למחצה. הפעלה בצורה קוואזי-תהודתית עם זמן פתיחה קבוע של המתג וזרם לא רציף בסליל הכניסה (DCM) גורמת לכך שמשפחת מעגלים זו מדמה נגד לרשת חשמל וכתוצאה משיגה גורם הספק קרוב ל-1 ועם עיוותים הרמוניים קטנים.

אבי טיפוס של המעגלים שנותחו הראו התאמה לתאוריה וסימולציה. גורם ההספק היה מעל 0.99 והעיוותים הרמוניים מתחת ל-5 אחוז בנקודות עבודה קרובות להספק נומינאלי של 20 וואט לשרשרת LED-ים.

אוניברסיטת תל-אביב

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דוחפי LED קוואזי-תהודתיים עם צימוד קיבולי

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על - ידי

אלכסנדר בזרוב

העבודה נעשתה בביה"ס להנדסת חשמל

במחלקה לאלקטרוניקה פיסיקלית

בהנחית דר' אלכסנדר אברמוביץ' ופרופ' דורון שמילוביץ

טבת תשע"ח

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